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Quadrature Power Amplifier for RF Applications

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Abstract

A new power amplifier (PA) architecture is proposed as a more power efficient way to amplify modulated signals at radio-frequencies (RF) compared to conventional polar power amplifiers.
Polar PA's, using the Envelope Elimination and Restoration (EER) linearizing technique for high efficiency switch mode amplifiers provide amplification for modulated signals at RF with high efficiency and linearity. However, such systems require high alignment between phase and amplitude signal paths and the bandwidth of the amplitude path needs to be three to four times the RF-bandwidth. The latter directly translates to high power consumption.
Instead of decomposing the quadrature signals to a phase and amplitude signal set, suggested is that the quadrature signals are to be directly amplified using a quadrature power amplifier. The lack of a separate phase and amplitude signal path avoids the linearity and bandwidth requirements, thus reducing power consumption.

A possible quadrature PA architecture is presented. This architecture consists of two supply modulated switch mode amplifiers placed in a bridge and is capable of handling negative voltages, modulation and power combining at RF. Furthermore, a driver architecture is presented to properly drive the quadrature PA.
Simulations results of the quadrature PA using 90nm CMOS models show a functional quadrature PA model with a power added efficiency of 30% at 6.4dBm output power driven at 2.4GHz and a maximum input power at 10MHz and 25% at 5.1dBm output power at 50MHz.

Preface

“If you just study long enough, eventually you don’t even know what a resistor is anymore”, said by Ir. M.G. “Rien” van Leeuwen during first year electronics course “EL-BAS”. Now, almost ten years ago and I found these words to be very true in the years to follow. Especially the last year, as I started working on my master assignment, till what is now this thesis, from time to time I “forgot what a resistor was”. And from there on in, the only way to avoid insanity is to go one or more steps back. In the end, I think this characterizes not only my master assignment, but my total study career at the University Twente; two steps forward and one step back.

Though slowly, but steady, always avoiding insanity, I could not have finished my master without the help of the people I met through the years. Especially this last year and I want to thank the people of floor 3, the ICD and SC people for their support, cheerful good mornings or colorful discussions about food, politics, music, motorcycles and sometimes electronics. I want to thank head of chair, Bram Nauta, especially for giving me the opportunity to go to Japan for my internship and my direct supervisor Ronan van der Zee for his seemingly endless patience. And last, but not least, I want to thank my fellow master students Pieter Koster and Mark Ruiter: take care of my plant, will you ?

Chen-Hai Li
“foxhole 3120”
18 November 2009

"*The more I learn, the more I realize I don't know*"
~Albert Einstein (1879 – 1955)

Contents

1. Introduction

For mobile communication systems the transceiver is the key block, for a transceiver, made up from the words transmitter and receiver, sends and receives signals to and from the antenna, making wireless communication possible. Early radio transceivers date from the 1900's, such as Hughes' Morse induction machine and Edison's broadcast over the Lehigh Valley Railroad. The following years, other researches including people like Hertz, Faraday, Maxwell and Tesla contributed to the theory of electromagnetism and wave-theory, making it possible for people like Armstrong, to construct transceivers concepts which are still used today.

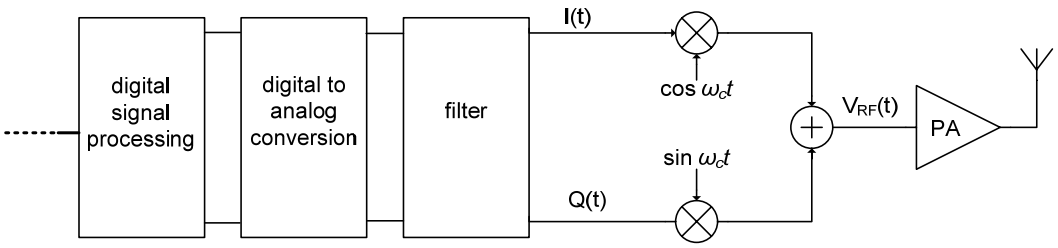

Figure 1 typical RF transmitter with direct conversion architecture

Pushed by the technological revolution of the past decades these wireless systems have evolved from simple Morse code transceivers to complex systems. With the help of digital computing on chip, complex (de-)modulation is possible, leading to quadrature up- and down-conversion architectures. A commonly used architecture is the direct conversion architecture as shown in Figure 1 [19][20].

Still, a power amplifier (PA) remains a power hungry block. In a time where smart usage of energy resources is not only cost wise, but also environmentally wise, the need for architectures with a less power consuming power amplifier is desired.

This thesis presents a new concept and model for a possible more power efficient power amplifier architecture. In the following chapter power amplifiers in general and linearization techniques are discussed. A step for step design that leads to a model for the quadrature power amplifier is given in chapter 3. Chapter 4 deals with specifications, simulations and results. Lastly, conclusions and recommendations are found in chapters, 5 and 6.

2. Power amplifiers

2.1. Introduction

In a RF transmitter, the message signal undergoes several steps such as digital signal processing, digital to analog conversion and filtering. The last step between up conversion of the baseband signal to RF frequencies and the antenna is the amplification of the signal. Specified for different communication standards, the signal has to be amplified to a certain power level so that it can be transmitted, received and decoded within a fixed geographical region. In contrast to small signal amplifiers, these amplifiers have to deliver serious amount of power, hence the commonly used term power amplifier (PA).

Traditionally power amplifiers (PA's) have been categorized in classes; A, B, C, D, E, etc. A second distinction can be made on the operating character of the active device: acting as a current source or as a switch. The "classic" classes A, B, A/B and C belongs to the first group. Classes D and E belong to the latter.

First the power efficiency of power amplifiers is discussed (§2.2). Following is an overview of the different classes and modes (§2.3 and §2.4). The discussion of the Envelope Elimination and Restoration (§2.5.1) and the Linear Amplification with Non-Linear Components (§2.5.2) linearization techniques concludes this chapter.

2.2. Efficiency

The conventional way of designing PA's is not to achieve maximum power transfer, but aiming for high efficiency. One might say that maximum power transfer makes logic sense, figuring the large amount of power needed to drive the antenna, but a PA with a conjugate match, the efficiency would be 50% maximum. Not only is this value unacceptable low, but also offers practical problems. An efficiency of 50% means that the same power dissipated in the load, will also be dissipated in the circuit. Considering the relatively large amounts of power needed to drive the antenna, this would give rise to thermal problems of the circuit itself. For nowadays applications such as cellphones and other portable communication devices this would be quite troublesome. [1][3]

Instead of aiming for maximum power transfer, PA's are designed for the highest possible efficiency while maintaining an acceptable gain and linearity. The

efficiency is therefore the performance parameters mostly used for power amplifiers. Two metrics for efficiency are used: drain efficiency, which is defined as the ratio between the power delivered to the load and the power delivered by the supply:

$$\eta = \frac{P_{out}}{P_{dc}} \tag{1}$$

Drain efficiency can give high efficiency for PA's that have no power gain. To overcome this, a second metric was introduced: power added efficiency (PAE). The power added efficiency is defined as the ratio between the difference of the RF output and input power and the power delivered by the supply.

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{2}$$

It can be seen that the PAE is lower than the drain efficiency. For PA's with relatively high power gains the PAE becomes equal to the drain efficiency.

2.3. Linear mode amplifiers

When the device acts as a current source, the transistor is biased in such a way that it drives in saturation. Sometimes called linear mode amplifier, however the input output relation can have a very non linear characteristic.

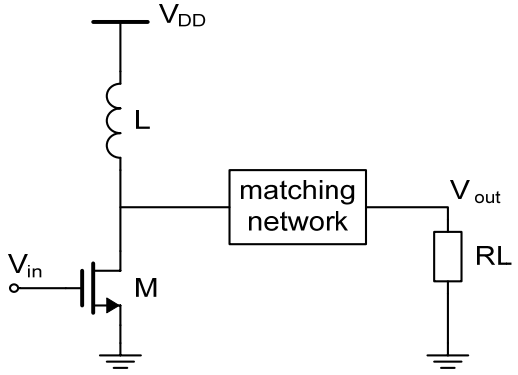

Figure 2 typical RF power amplifier configuration

Power amplifiers for RF with the transistor acting as a current source all have the same basic circuit. In this general model, shown in Figure 2, the output power is delivered to the load, modeled by resistor R_L. A "big" inductor or radio-frequency choke (RFC) approximates the behavior of a current source. Dependent of operation

and application a load network is used e.g. to shape signals or use impedance transformations to maximize power efficiency. Historically, power amplifiers are primarily distinguished in terms of which part of the RF input cycle the transistor conducts. This conduction angle classifies linear mode amplifiers in classes A, B, AB and C.

2.3.1 Class A

A class-A power amplifier can be regarded best as a textbook small signal amplifier suited for large signals. As shown in Figure 3, the transistor is biased in such a way that it is active for the total RF cycle: the conduction angle for a class-A PA is 360°.

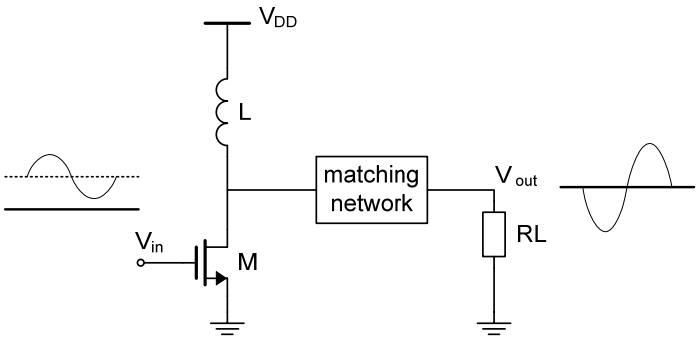

Figure 3 typical class-A power amplifier configuration

The transistor is biased depending on its input as the bias voltage is set so that the corresponding output will never turn the transistor off. The output swing is therefore maximized while providing high linearity and high gain.
However the class-A PA has a constant quiescent current even when there is no signal. Also, to reduce distortion large currents and high voltages are needed. This results in high power consumption. The power efficiency of a class-A PA is therefore quite low. The theoretical maximum efficiency is 50%, in practice 35% and when really high linearity is needed, the efficiency is lower than 25% [1].

2.3.2 Class B

To improve the power efficiency of a class-A PA, the transistor can be made active for only half the RF cycle. Such is the case for a class-B PA as shown in Figure 4. The transistor is biased at the cut-off voltage; there is zero quiescent current. Since the conduction angle is 180°, class-B amplifiers are mostly operated in push pull configuration. The two drain currents together produce the full RF-cycle.

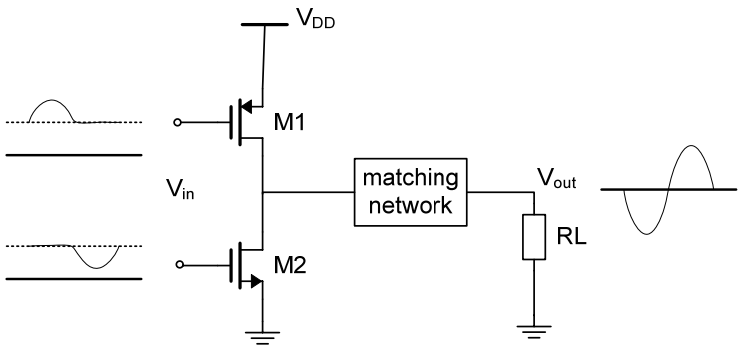

Figure 4 typical class-B power amplifier in push-pull configuration

Having simultaneously a drain current and voltage of zero for a fraction of the RF cycle, thus reducing transistor dissipation, increases the efficiency. For a class-B, the theoretical efficiency is 78.5% [1][3]. However, such high efficiency is only at maximum output power. Overall efficiency will be lower for transmitting at less than maximum power. Though a class-B amplifier has improved power efficiency regarding to class-A amplifiers, the costs is less linearity [4].

2.3.3 Class AB

A class AB is the best of both worlds. Its configuration is a class-B PA, but instead of biasing the transistor at cut-off, a small fraction of bias currents is allowed. Thus while maintaining efficiency approximating class-B, a linearity approximating class-A is achieved. Depending on the linearity and efficiency requirements the bias level of the class-AB PA is determined.
Theoretically the efficiency and linearity performance depending on bias level, can be anything in between full class-A or full class-B.

2.3.4 Class C

As in class-B, the power efficiency of a class-C is increased by reducing the conduction angle. Its configuration is quite similar as a single transistor class-B amplifier, however a class-C can have a conduction angle as low as 0°. As the conduction angle decreases, the transistor is on for a smaller fraction of the RF cycle, reducing power dissipation. Theoretically the power efficiency is, as for class-B, 78.5% for a 180° conduction angle to 100% for a 0° conduction angle. However for a 0° conduction angle the power to the load also drops to zero. This means that a class-C can only have high efficiency if it delivers power for a fraction of the of the peak output power. Therefore a class-C is not suitable for portable devices where efficiency at full power is important. [1][3]

2.4. Switch-mode power amplifiers

In switch-mode amplifiers the active device acts as a switch. The idea behind using switches is that an ideal switch doesn't dissipate power, for there is either zero voltage across or zero current through the switch. Thus the voltage-current product is zero, the transistor dissipates no power and efficiency is 100%. This is shown in Figure 5.

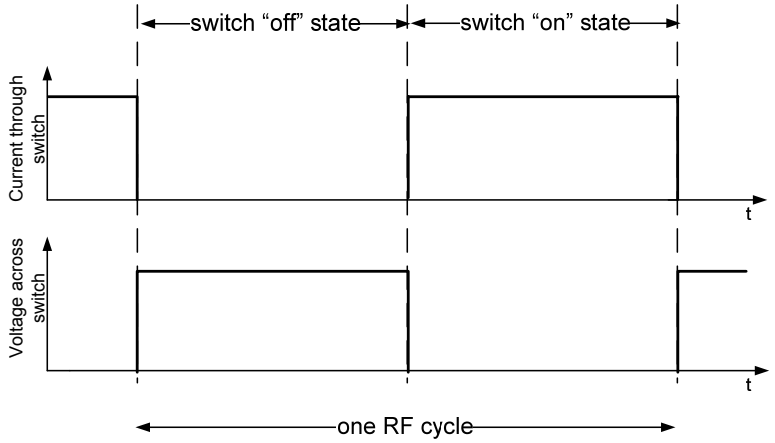

Figure 5 voltage and current relation of an ideal switch-mode transistor

Unlike linear-mode power amplifiers the output signal is not intended to be a replica of the input. Thus not the conduction angle, but the way the voltage and current waveforms are shaped is the primary distinction between the switch-mode power amplifiers classes. Of the three conventional switch-mode PA classes; class D, E and F only the first two are discussed.

2.4.1 Class-D

Class-D consists of a pair of active devices and a tuned load network. The active devices act as a switch in such a way that the generated output is defined as a rectangular voltage waveform. The tuned output circuit acts as a filter tuned to the switching frequency and removes its higher frequency components, resulting in a sinusoidal output. Since the transistors are switching between ground and the voltage supply, the output is directly linked to the supply, making class-D very suitable for voltage supply modulation.

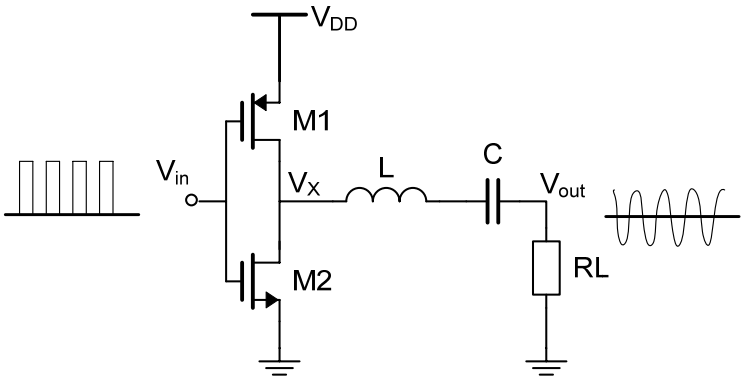

Figure 6 typical class-D power amplifier configuration

Figure 6 shows a basic class-D circuit, NMOST and PMOST transistors act as a switch like an inverter output stage, switching between the supply and ground, generating a rectangular voltage waveform. An LCR network acts as the tuned output filter. A properly tuned load network will have a low reactance to the fundamental and high impedance for the harmonics, resulting in a sinusoidal output across the load. This load, i.e. the antenna is modeled by resistance R_L.

The transistors operate in a push pull configuration, similar to class-B, but are driven so hard that they operate as switches. A gate bias is not needed, but the input signal must be sufficient to drive the transistors in triode and cut-off at the right time of the RF-cycle.
Ideal switches dissipate no power due to infinite switching time. A tuned LC network doesn't dissipate power as well. Thus, theoretical the efficiency of an idealized class-D PA is 100%. However ideal switches do not exist. Real switches exhibit finite switching time. Such real life devices will exhibit time overlap between voltages across and current through the switches, dissipating power, reducing efficiency. Furthermore, conduction losses in transistor on-resistance and component resistance as well as capacitive switching losses due to drain capacitances will reduce the efficiency even more.

2.4.2 Class E

The class-E concept has been first introduced by Ewing in 1964 in his doctoral thesis and has been significantly developed by the Sokals and others in the seventies. In a class-E configuration, the active device operates as a switch and a passive load-network shape the voltage and currents waveforms in such a way that there is no simultaneously overlap between voltage across and current trough the transistor. The result is a "soft" switching of the transistor to ensure no voltage and current overlap as is the case with "hard" switching for class-D.

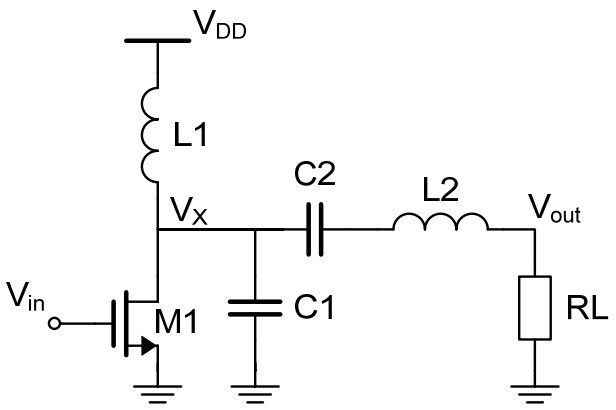

Figure 7 typical class-E power amplifier configuration

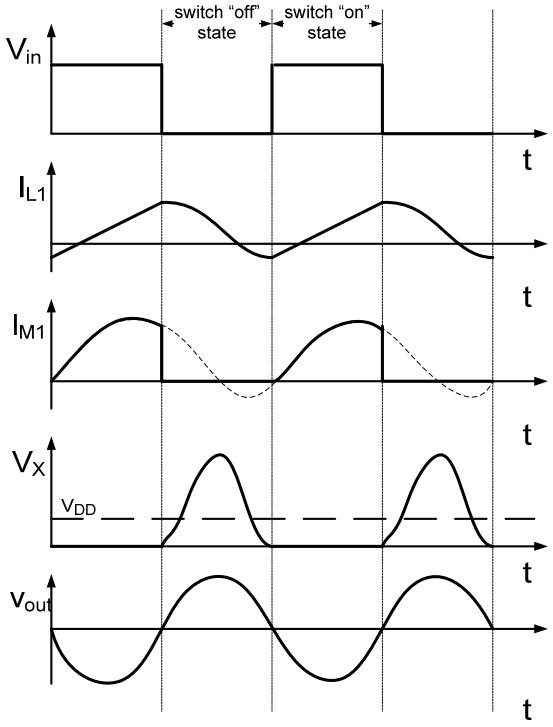

Figure 8 typical voltage and current waveforms for a class-E PA

Figure 7 and Figure 8 show the classic class E circuit and its typical waveforms. The amplifier consists of a switched operated transistor that is "on", with no voltage across it, or is "off", with no current through it. The radio frequency choke (RFC) is assumed large enough so that the current I_L flowing through is constant. The quality factor of the tuned output network is assumed high enough that the output signal is sinusoidal. An advantage of the class-E design is its straight forward designing with little post design tuning. The values of the load network are chosen in such a way

that the voltages across and currents trough the active device satisfy a set of conditions; 1) At the turn off state, V_X is delayed until the current drops to zero, 2) At the turn on stage, V_X returns to zero, before the current increases and 3) the slope of V_X is near zero at the turn on stage of the switch. The result is that the waveforms never have simultaneously high voltage and high currents. This yields in lower power dissipation, thus a higher efficiency.
The derivation of the design equations can be found in [6] and a more elaborate discussion and more specific approximation in [5]. The basic forms are as follows:

$$R = \frac{V_{DD}^2}{P}\left(\frac{2}{\frac{\pi^2}{4}+1}\right) = 0.577\frac{V_{DD}^2}{P}$$

$$L_2 = QR/2\pi f$$

$$C_1 = \frac{1}{2}\pi fR\left(\frac{\pi^2}{4}+1\right)\left(\frac{\pi}{2}\right) = \frac{5.447}{2}\pi fR$$

$$C_2 \approx \left(\frac{1}{(2\pi f)^2 L_2}\right)\left(1+\frac{1.42}{Q-2.08}\right) \qquad (3)$$

The R denotes not only the load resistance, but the total resistance in the system, P the wanted output power and Q denotes the quality factor of the load network.

Though the voltage has zero slope at turn off, the current is almost maximum. It is shown that the peak drain current is roughly $1.7V_{DD}/R$. [3][4]. This means that if the switch is not fast enough, there is still high switch dissipation. Also, a real switch exhibits an on-resistance. In practice this means that a switch has a nonzero "on" voltage.
Another property of the class-E PA is that it exhibits a large peak voltage in the off state approximately $3.56V_{DD}$-$2.56V_{min}$, with V_{min} the minimal voltage across the transistor. This demands the usage of devices with a higher breakdown voltage than the voltage given for used technology. Because of afore mentioned reason, a class-E is quite demanding of its switch specifications.
The advantage of class E is the high efficiency, theoretically approaching 100%. Also, the drain source capacitance of the transistor can be used as the shunt capacitor. In other words, power loss can be reduced, since the transistor's capacitance is not a source of power loss as in the case with class-D, but a part of the loading network.

2.5. Linearization techniques for power amplifiers

As the most efficient power amplifiers are normally nonlinear, the needs for linearizing techniques arise in many RF applications to restore linearity. Two linearization techniques will be shown in the following paragraphs: envelope elimination and restoration (EER) and linear amplification using non-linear components (LINC). The first will be the direct motivation for the quadrature power amplifier architecture to be presented in chapter 3. The latter shows several concepts which show similarities with the presented power amplifier and is therefore mentioned.

2.5.1 Envelope Elimination and Restoration

Envelope Elimination and Restoration (EER) was first proposed by Kahn in 1952 and is also called polar modulation. The basic principal is that bandpass signals can be regarded as a result of amplitude modulation and phase modulation. This can be seen by describing a modulated RF signal in terms of quadrature signals:

$$Vrf(t) = I(t)\sin(\omega t) + Q(t)\cos(\omega t) \qquad (4)$$

Defining the quadrature components I(t) and Q(t) as:

$$I(t)=A(t)\sin(\phi(t))$$
$$Q(t)=A(t)\cos(\phi(t))$$

and

$$A(t) = \sqrt{I^2(t) + Q^2(t)}$$
$$\phi(t) = \arctan\frac{Q(t)}{I(t)}$$

This leads to:

$$Vrf = A(t)[\sin(\phi(t))\sin(\omega t) + \cos(\phi(t))\cos(\omega t)] \qquad (5)$$

From this follows the general form of a modulated signal:

$$Vrf(t) = A(t)\sin(\omega t + \phi(t)) \qquad (6)$$

In this form A(t) is the amplitude modulation and φ(t) the phase modulation of the signal.
An EER PA first separates these two signals, while at the PA level modulation is used to combine these signals to regain the original bandpass signal. Such EER PA's are designed to provide high power efficiency for amplitude modulated signals.

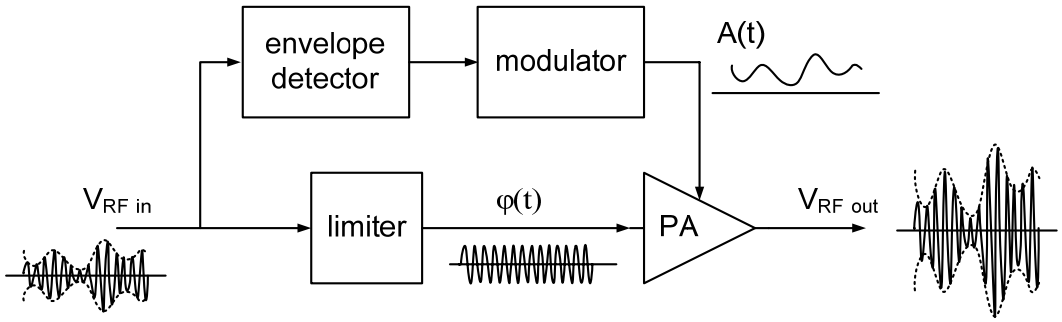

Figure 9 envelope elimination and restoration

Figure 9 illustrates this concept. An RF bandpass signal drives an envelop detector and a limiter, such that the amplitude and phase signals are separated. Each signal is amplified and combined in the PA, hence the name envelope elimination and restoration. If a switch mode PA, i.e. class-D or class-E is used, the output current flowing through drain is a direct function of the envelope, thus the supply of the PA is modulated with the amplitude. Because of the constant amplitude of the phase signal φ(t), the phase information will hardly be distorted by the non-linear amplifier. A transistor operating as a current source transistor is not suitable for amplitude modulation using voltage supply modulation, because the current is not a direct function of the voltage supply. [1][3].

The advantage is that a polar modulator requires less linearity at the PA level, since the linearity requirements are shifted to the amplitude path and the phase path. However, several other requirements are needed to prevent linearity degradation. The first is the need for a low differential delay between the amplitude and phase signal path. The envelope and phase signal have each their own path, operating at their own frequencies. A mis-timing of both signal paths in the PA modulator gives rise to distortion [10][11].
Secondly, a large bandwidth of the envelope modulator is needed. A finite bandwidth unwantedly corrupts the envelope signal. As illustrated in Figure 10, when the envelope signal reaches zero level, the waveform steepens, indicating a high frequency component. If the amplitude modulator has a finite bandwidth, this high frequency component will be filtered out, resulting in a smoothened envelope signal, noted by the dotted line. It is also shown that a large bandwidth of the envelope, with respect to the phase increases the carrier to intermodulation ratio of the third order intermodulation. With other words, increasing the bandwidth decreases the dominance of the third order intermodulation product. An envelope modulator bandwidth of 4 -10 times the envelope bandwidth is needed [2][10][11].

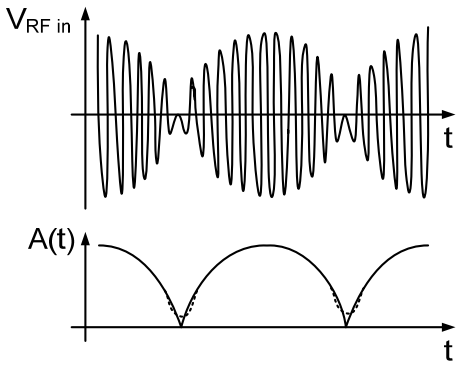

Figure 10 input and envelope signal in an EER system. The straight line corresponds with ideal behavior, the dotted line with finite envelope modulator bandwidth

Though EER loosens the linearity requirements of the PA, the PA still deals with issues such as AM-PM conversion due to drain capacitances and the modulating drain voltage of the transistor, as well as AM-AM conversion due to on-resistance of transistors. A short overview of several polar PA's found in literature are shown in Table 1.

reference	year	technology	application	PAE	peak output power
[8]	1998	0.8mm CMOS	800-900 MHz	49%	29.5 dBm
[9]	2005	GaAs HFET	2.4 GHz	28%	19 dBm
[15]	2005	0.18µm CMOS	1.75 GHz GSM-EDGE	34%	27 dBm
[7]	2008	5W LDMOSFET	1 GHz	39.5%	31.7 dBm
[16]	2008	GaAs MESFET	1 GHz	68%	27 dBm

Table 1 overview of polar designs in literature

2.5.2 Linear Amplification with Non linear components (LINC)

The Linear amplification with non linear components (LINC) or outphasing power amplifiers were first developed by Chireix in 1935. The principle is to vectorize the output signal in two, constant amplitude, phase modulated signals. Each signal is amplified individually and recombined.

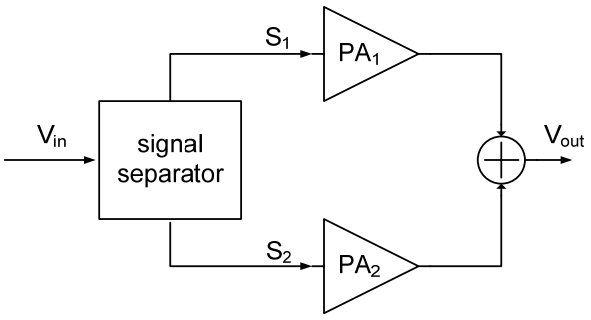

Figure 11 linear amplification using non-linear components

Figure 11 shows a block diagram of a possible LINC implementation. First the RF signal decomposed in two vector signals. Figure 12 shows the signal constellation for this situation. The two vectors signals S_1 and S_2, are constant amplitude, phase modulated. Each signal is amplified with two identical amplifiers. After recombining, the result is the sum of the two vectors, producing an amplified output signal.

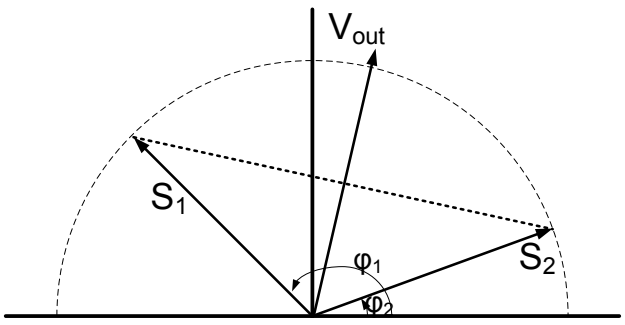

Figure 12 typical signal composition for LINC PA

Though LINC avoids the amplitude variation problem in a PA, it has a few drawbacks. First is the generation of the two vector signals S_1 and S_2. These are phase modulated with $\varphi(t)$, while this is a non-linear function of the amplitude. Two other issues are that gain and phase mismatch between the two signals paths generate residual distortion and the output is highly sensitive to the output angle. Lastly, the output combiner, in practical situation still gives significant losses. [1]

3. Quadrature Power Amplifier

3.1. Introduction

Envelope elimination and recombination offers a linearization technique to optimize power amplifiers in for example a direct conversion PA system to handle amplitude modulated signals with higher power efficiency. However, drawbacks such as differential delay in the signal paths and the bandwidth requirements for the envelope, as well as linear requirements for the switch-mode amplifier can degrade performance. Also, the design is not so straightforward since it needs several operating blocks such as an envelope detector, envelope modulator and a limiter.

A possible way to overcome these problems is to operate the PA in a quadrature configuration. Instead of decomposing the quadrature signals to a phase and amplitude signal set, the quadrature signals are to be directly amplified and modulated using a quadrature power amplifier. The lack of a separate phase and amplitude signal path avoids the linearity and bandwidth requirements

In the following paragraphs this concept is explored, discussing the basic idea and choice of PA class to start with (§3.2 & §3.3). Following is a detailed discussion about modeling and designing the quadrature power amplifier architecture (§3.4, §3.5, §3.6 and §3.7). About losses and sizing of the final architecture can be found in §3.8 and a short word on AM-PM distortion can be found in §3.9. The final paragraph deals with the driver architecture to proper drive the quadrature PA (§3.10).

3.2. Quadrature signals and quadrature PA concept

As shown in §2.5.1, the general form of a modulated signal is described as:

$$Vrf(t) = A(t)\sin(\omega t + \phi(t)) \tag{7}$$

But written as:

$$Vrf(t) = A(t)\cos(\omega t + \phi(t)) \tag{8}$$

the modulated RF signal can be written as:

$$Vrf = A(t)[\cos(\phi(t))\cos(\omega t) - \sin(\phi(t))\sin(\omega t)] \tag{9}$$

using

$$I(t)=A(t)\cos(\phi(t))$$
$$Q(t)=A(t)\sin(\phi(t))$$

resulting in:

$$Vrf(t) = I(t)\cos(\omega t) - Q(t)\sin(\omega t) \qquad (10)$$

This result shows that a modulated RF signal can also be expressed as a subtraction of two modulated quadrature signals I(t) and Q(t). This is valid as since both (7) and (8) can be used to describe modulated signals.

Figure 9 shows a possible block diagram of such quadrature modulator scheme. Two message signals, I(t) and Q(t) are mixed with a local oscillator with a 90° phase shift with respect to each other. A subtraction is used to obtain the signal as according to *(10)*.

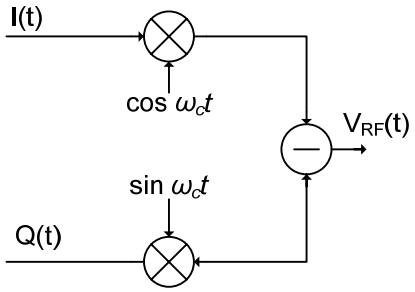

Figure 13 quadrature modulator

Though more common as addition as in *(4)*, this concept of quadrature modulation can be found in widely used systems as digital modulation schemes and correlation receivers and can be extended to power amplifiers.

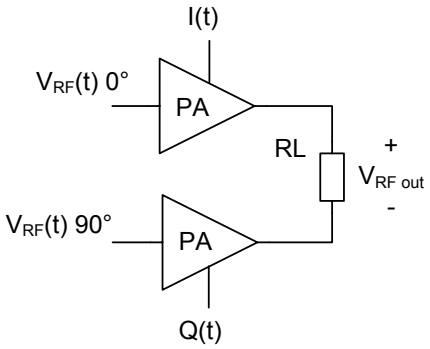

Figure 14 quadrature power amplifier

Figure 14 shows this concept for a power amplifier system. The most basic form consists of two quadrature modulated PA's, 90° phase difference in bridge mode. Unlike traditional EER, each PA amplifier is driven by constant amplitude, constant phase, carrier signal and the voltage supply is modulated with either I(t) or Q(t) signal. The load in the bridge, e.g. an antenna senses the difference between the modulated outputs of each PA, thus a subtraction is realized.

Since each PA is driven by a constant amplitude and constant phase RF carrier signal, only the quadrature signals I(t) and Q(t) contains information. This eliminates the need for matching between an envelope and a phase paths as is the case for conventional EER.
Secondly, since there is no envelope path that has to match with a much higher bandwidth phase path, the need for a wideband envelope path is redundant. This implies, that the bandwidth of the signal in a quadrature PA system, determined by the quadrature signal I(t) and Q(t), is much lower than the limited bandwidth of the envelope modulator as with an EER system.

The output voltage as seen at the load terminals can easily be predicted using an I-Q constellation diagram. Shown in Figure 15, mapping the I(t) waveform on the y-axis and the Q(t) waveform on the x-axis, the resulting envelope output amplitude and phase of the RF carrier signal can be reconstructed. Suppose I(t) and Q(t) are sinusoid with 90° phase difference, the resulting output will be an RF carrier signal with a constant amplitude.

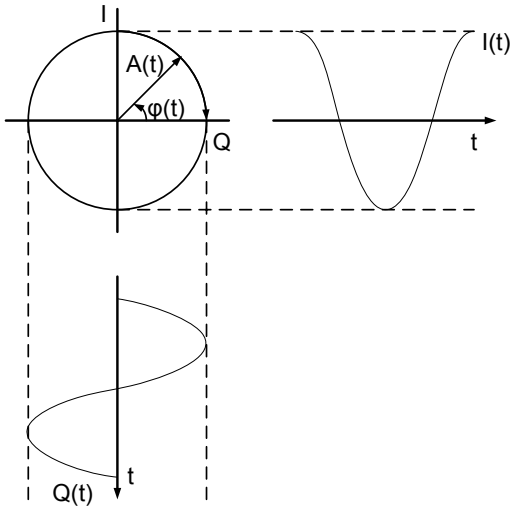

Figure 15 quadrature signal constellation

Such an operation causes the output to shift up in frequency. Shown in Figure 16 is the power spectrum of RF carrier, the quadrature signals and the resulting input signal. Suppose, as in Figure 15, I(t) is cosinusoid and Q(t) is sinusoid. Since the quadrature PA has a mixing characteristic, the quadrature signals are translated to

the RF frequency. As the quadrature signals differ 90° in phase, the negative frequency component is cancelled out. This results in a single sideband carrier suppressed (SSSR) modulation, which in this case as mentioned, is a single frequency shifted up with the quadrature bandwidth.

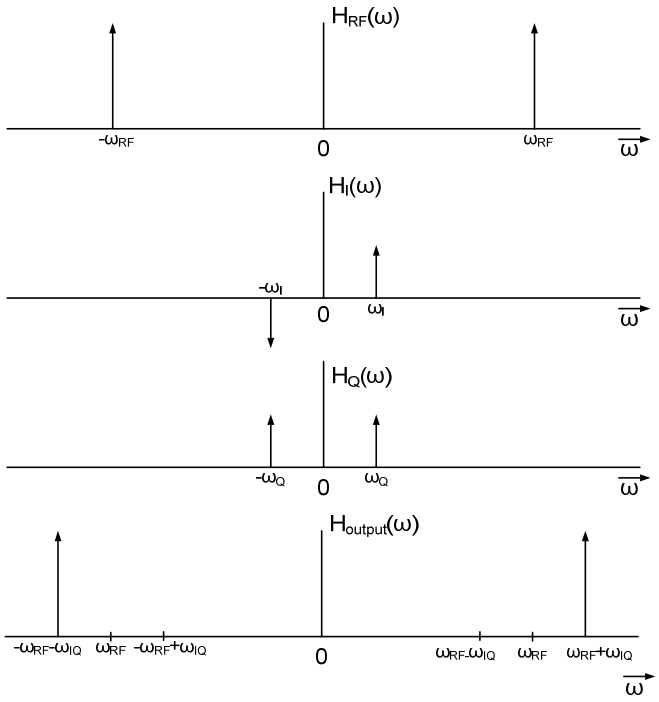

Figure 16 spectrum of the RF signal (H_{RF}), sinusoidal quadrature signals (H_I and H_Q) and the resulting output (H_{output})

The downside of using a quadrature configuration is the mismatch between the I- and Q side in amplitude or phase. The result is a corrupted reconstruction of the RF message signal, downgrading overall performance. This mismatch can happen at several stages in the transmitter. At the power amplifier stage mismatch could occur for example when the RF input is multiplied with the quadrature signals resulting in amplitude mismatch or difference in path lengths resulting in phase mismatch.
On the subject of quadrature mismatch much is written and numerous techniques can be found in literature which have reasonable results [21][22][23].
Quadrature mismatch is thus a quite common problem, but just as all mismatch related problems, doesn't need to be a limiting factor to forsake the use of quadrature architectures.

A second downside using a quadrature configuration is the need for a power combiner. In the model of Figure 14, the subtraction of the two mixing PA's a resistor is used. This resistor models the antenna, but in practice an antenna is not a two terminal component that can be connected as a resistor. A power combiner will be needed to subtract the signals and the resulting output has to drive the antenna.

Just as in Linear Amplification Using Non Linear Components (LINC), such a power combiner is a critical stage in the design, since a quadrature PA will also be sensitive to mismatch between the two signal paths.
Regarding power combiners, a limited number of articles can be found in literature. Most of the mentioned techniques use either quarter wave length transmission lines or transformers. The use of the former changes the voltage character of a system output to a current character. The result is that output of the different stages can be connected if it were current sources. The downside is that a quarter wavelength is impossible to implement on-chip. The use of transformers has a more widespread use operating at the gigahertz region. However to keep losses at a minimum, a high quality factor of the transformer is needed. This will mean that the components are relatively big, consuming major chip area or give rise to the need for using off-chip components.
Additionally, besides power combining, a transformer can also operate as impedance transformation. This will make the use for lumped LC impedance transformation network superfluous [24][25][26][27].

3.3. Choice of PA configuration in quadrature PA system

In a quadrature PA system as described in the previous paragraph, the PA modulates an RF carrier signal with the quadrature signals I(t) and Q(t). The simplest way to achieve this is to use a switch mode amplifier such as class-D or class-E. These configurations are easily suitable for supply voltage modulation. Driving the amplifier with a hard switching RF signal and using the quadrature signal as supply voltage should generate the wanted modulated RF signal.
Supply modulation using a linear mode amplifier such as class-A or class AB, would be impossible since the output current is not a direct and linear function of the voltage supply. Modulating and driving such PA configuration would involve a more complicated configuration.

Of the two switch mode power amplifiers, the class-E favors because of its higher efficiency. However, it is unusable in a quadrature bridge configuration. Suppose the single end class-E power amplifier model using ideal switches with infinite high open resistance, neglectable low closed resistance of 1mΩ, no parasitic switch capacitances and infinitely small switching times. The switch is driven with a hard switching, 2.4Ghz, 50% duty cycle, RF pulse signal and the supply is connected to V_{DD}=1.2V. The output should thus be a sinusoid with amplitude V_{outI}=1.2V. The RF-choke inductor L_1 is assumed to be large enough, the wanted output power is P_{out}=1W and the quality factor of the tank is Q=10. The component values are found using the Sokal formulas of *(3)* as given in §2.4.2 and are listed in Table 2.
The characteristics waveforms are shown in Figure 18 and correspond to the characteristics as found in §2.4.2.

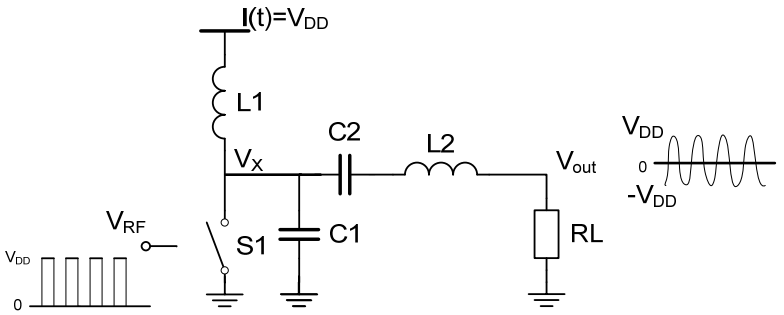

Figure 17 single end class-E PA

component	value
L_1	5nH
L_2	525pH
C_1	16.6pF
C_2	0.93pF
R_L	790mΩ

Table 2 component values of a single end class-E PA.

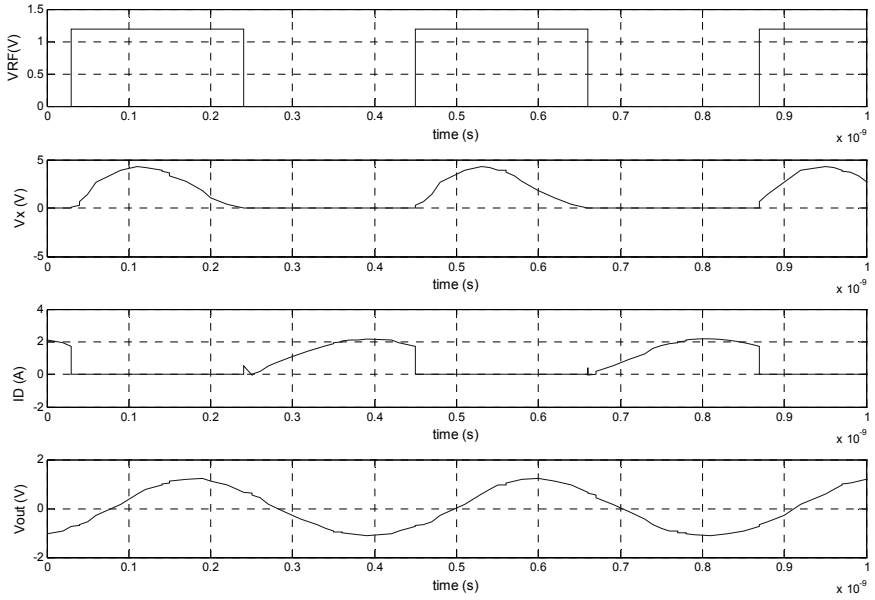

Figure 18 tuned single end class-E PA waveforms

Now, suppose the configuration of Figure 19. Using two identical class-E amplifiers of Figure 17 and placed in a bridge. Again, each side is driven with a hard switching, 2.4Ghz, 50% duty cycle, RF pulse signal but the right, Q(t)-side of the bridge lags 90° in phase in respect with the left, I(t)-side. The supply is modulated with a constant supply voltage at V_{DD}=1.2V. The output across the load R_L, between the nodes V_{outI} and V_{outQ} should be a sinusoid with constant amplitude of $\sqrt{(V_{DD}^2+V_{DD}^2)}$.
The RF-choke inductors L_1 and L_3 are assumed to be large enough, the wanted output power is P_{out}=1W and the quality factor of the tank is Q=10. The components value are found using the Sokal formulas of *(3)* as given in §2.4.2 and are listed in Table 3.

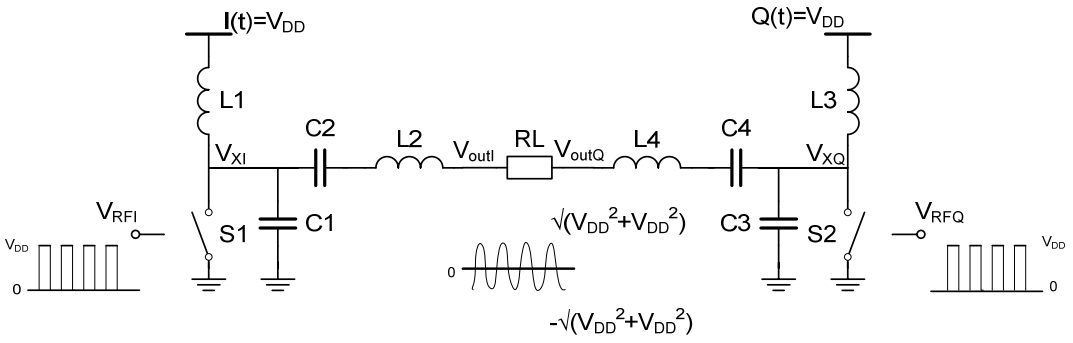

Figure 19 ideal operation of a class-E power amplifier using ideal switches in bridge mode

component	value
L_1 L_3	5nH
L_2 L_4	525pH
C_1 C_3	16.6pF
C_2 C_4	0.93pF
R_L	790mΩ

Table 3 component values of Class-E PA in bridge mode

Compared to the waveforms of a single end class-E power amplifier, the waveforms of the bridged class-E power amplifier show differences, while they should be the same. Both the left as the right side show not the correct voltage and current waveform characteristics as in Figure 18. Furthermore, both sides don't show equal waveforms. The result is not the expected voltage waveform across the load.

This behavior can be attributed to the fact that, though the load will sense the difference of both output voltages, the output current will be added. This nett current will have to go to either the left or right side since there is no path to

ground. This would be no problem if the class-E amplifiers would have a voltage source characteristic, but they tend to have a more current source characteristic due to the RF-choke.
This is made evident as the current through switch S2 is negative, indicating that the current is flowing in opposite direction. This results from the aforementioned nett current forced to either side in the bridge In this case to the right side, since the I(t)-side leads and Q(t)-side lags. Reversing the phase difference, results in that the nett current will flow to the left or I(t)-side.

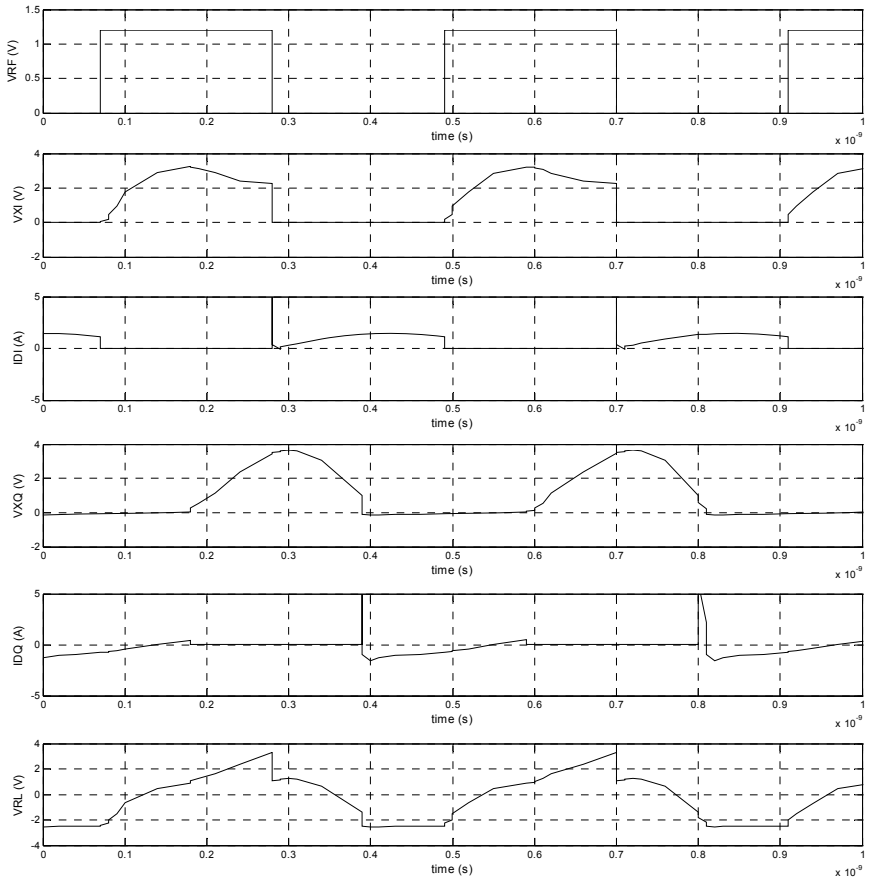

Figure 20 waveforms for two class-E PA in bridge mode

Also, as shown in [5] the voltage at V_{XI} indicates at a too low value for C1 and C2, while the voltage at V_{XQ} indicates a too high value for C3 and C4.
A nett-current in bridged class-E PA leads thus to unexpected voltage-current relation with non-tuned components. This results in the output voltage across the load, V_{RL} as shown in Figure 20. It shows a waveform that not even resembles a sinusoid.

A class-D however, does have a voltage source characteristic. A nett-current can flow back to the voltage supply and will not encounter these problems. In other

words, a class-D will be suitable to operate in bridge mode for a quadrature PA system.

3.4. Quadrature PA model with switches

As shown, a quadrature power amplifier is configured as two voltage supply modulated switch-mode power amplifiers placed in a bridge, operating at 90° phase difference. A class-E is unsuitable, but a class-D is, because its voltage characteristic enables any nett current caused by the 90° phase difference to flow back in the supply. Therefore, the class-D architecture will be the basic form of the quadrature power amplifier model.

In a class-D PA the transistors operate in switch-mode. The PA can therefore easily be modeled with switches. Using ideal switches with infinite high open resistance, neglectable low closed resistance, no parasitic switch capacitances and infinite switching times, a first order model can be realized omitting all high order effects. This is done to gain a principle insight of the operation of the quadrature PA.

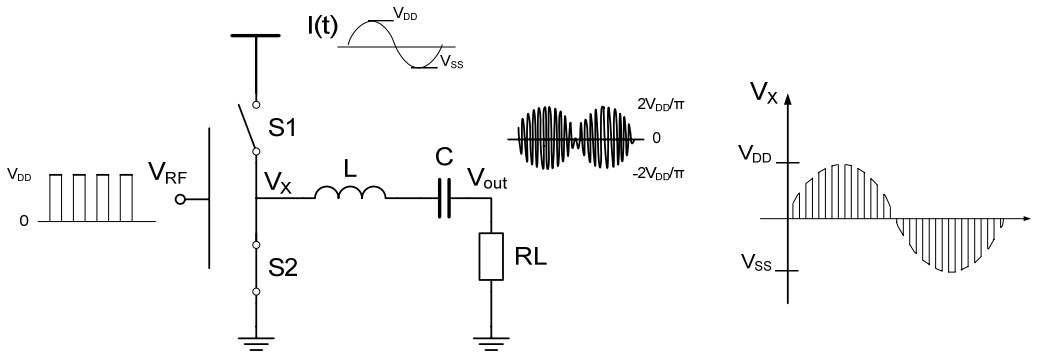

Figure 21 single end quadrature power amplifier using ideal switches

Using ideal switches, the modulating switching PA can be modeled as Figure 21. As a quadrature PA needs two amplifiers in bridge mode, a single amplifier will be denoted as a single end quadrature PA. Operating as a class-D, the PA is driven with a hard switching RF signal, between zero and V_{DD}=1.2V, with a duty cycle of 50% in such a way that either one switch is open and the other closed or vice versa, but never open or closed simultaneously. If the RF signal is zero the output is connected to the supply rail and if V_{DD}, the output is connected to ground. The supply is modulated with a baseband quadrature signal I(t), which in this case is sinusoid with from V_{DD}=1.2V to V_{SS}=-1.2V. The result at node V_X is an RF pulse signal multiplied with the voltage supply; its envelope is a replica of the modulating signal I(t).

Just as for a conventional class-D PA, a tuned network is used to produce a harmonic waveform across the load, modeled by resistor R_L. For this network, again just as in a conventional class-D PA a first order LC network can be used, as shown in Figure 21.

The filter is tuned to the RF frequency according to:

$$\omega = \frac{1}{\sqrt{LC}} \tag{11}$$

The quality factor of a series LCR network is defined as the ratio of energy stored to the energy lost per unit time and can be expressed as:

$$Q = \omega \frac{L}{R} \tag{12}$$

Another definition of the quality factor is the steepness of the frequency response of the filter. An LCR filter thus resonates at the tuned frequency and usually exhibits a bandpass transfer function. The quality factor is the ratio between the tuned frequency and the -3dB bandwidth.

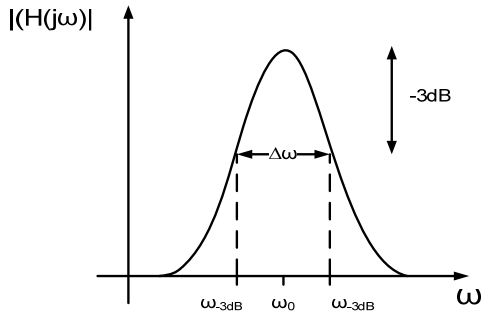

Figure 22 frequency response of LCR network

A too low Q can result in a low suppression of the higher harmonics, a too high a Q can result in large inductorvalues. A large inductor is not only difficult to make on-chip, but will also mean higher component resistance resulting in lower power efficiency. Furthermore, for a series LCR network at resonance, the voltage across the inductor or capacitor is Q times as great as that of the resistor. To limit these high voltages in the system it is preferable to keep the Q at minimum [3].

Using *(11)* and *(12)*, the filter can be dimensioned. The only free parameter to choose is the quality factor Q, L and C, since the resistor R_L models the 50Ω antenna and the RF frequency is set by applications standards (using the IEEE 802.11 standard) at f_{RF}=2.4GHz.

For simulation purposes a quality factor of 10 is sufficient. In practice, on-chip a lower quality factor is more common due to restricted area available for an inductor. The value used for the inductor as found and used is therefore also too high and not possible to create on-chip. Still, a quality factor of 10 is used as a starting point for the model for the sake of convenience. This value can be tweaked later on to accommodate a more practical on-chip inductor.
Another possibility is to use a smaller load and thus smaller inductance values while keeping Q constant. Shown here is a 50Ω resistance operating as power combiner, but using a transformer as power combiner and impedance transformer as described in §3.2, a smaller load can be used.
Using Q=10 and *(11)* and *(12)*, the values for the inductor and capacitor are:

$$L=33nH$$
$$C=0.133pF$$

A first order LC filter will have a low reactance to the fundamental and high impedance for the harmonics, resulting in a sinusoidal output. Assuming its input a 50% duty cycle, pulse signal, the Fourier series of said input is:

$$V_{out} = \frac{2V_{DD}}{\pi}\sum_{k=1}^{\infty}\frac{\sin((2k-1)2\pi ft)}{2k-1} = \frac{2V_{DD}}{\pi}(\sin\omega t + \frac{1}{3}\sin 3\omega t + \frac{1}{5}\sin 5\omega t + \cdots) \quad (13)$$

The fundamental at the output is thus a sine wave with a maximum amplitude of $2*V_{DD}(t)/\pi$. This implies that the output for a single end configuration as in Figure 21 will have a maximum amplitude of $2*I(t)/\pi$, with I(t) being the voltage supply modulated quadrature signal input. However, this is the case for a strict ideal pulse waveform as input. In practical this waveform is more a trapezoid. It is shown in [2] that the maximum amplitude is decreased as function of the rising and falling flanks of the input signal

Using the model of Figure 21 and the above mentioned specifications of the filter, Figure 23 shows simulation waveforms. The switches are driven with a hard switching RF pulse signal between zero (ground) and V_{DD}. For the supply I(t) a sinus at 50MHz is used with an amplitude of V_{DD}.

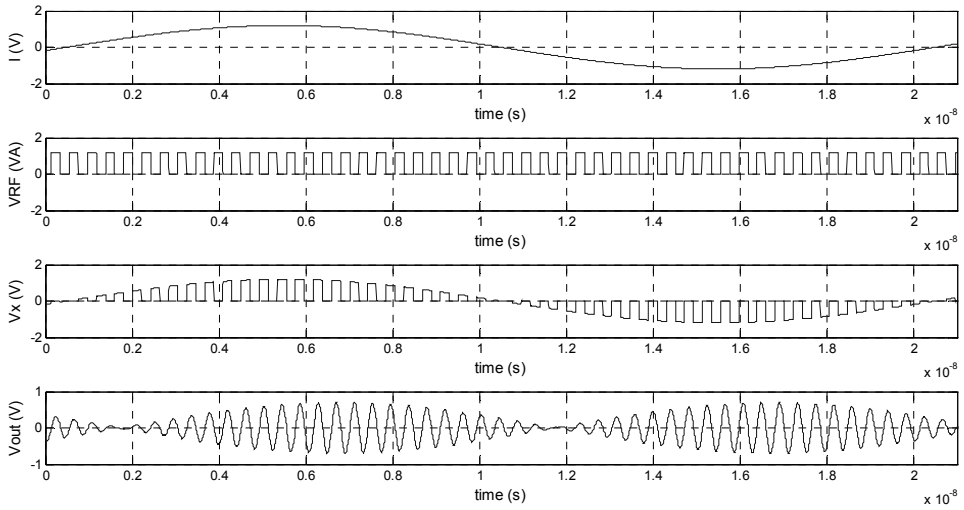

Figure 23 RF input signal and output voltages V_X and V_{out} of a single end quadrature PA using ideal switches

The resulting waveforms show indeed that at node V_X the RF signal is multiplied with the supply. At the output, this signal is filtered, resulting in a sinusoid with the same shaped. The maximum amplitude V_{out}=576mV and is smaller than the theoretical maximum, because of the bandpass characteristic of the LCR filer.

Figure 24 shows two identical modulating switching PA's in bridge mode. The load R_L is placed in between, resulting in the difference of the two output voltages across the load. The left side of the bridge is driven by hard switching RF signal and modulated with I(t), the right side is driven by the same hard switching RF signal, only 90° in phase delayed and is modulated with Q(t).

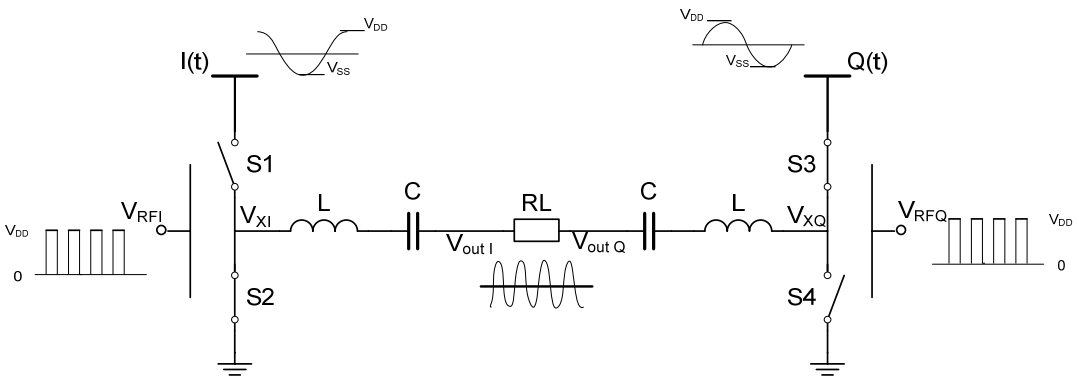

Figure 24 quadrature power amplifier using ideal switches

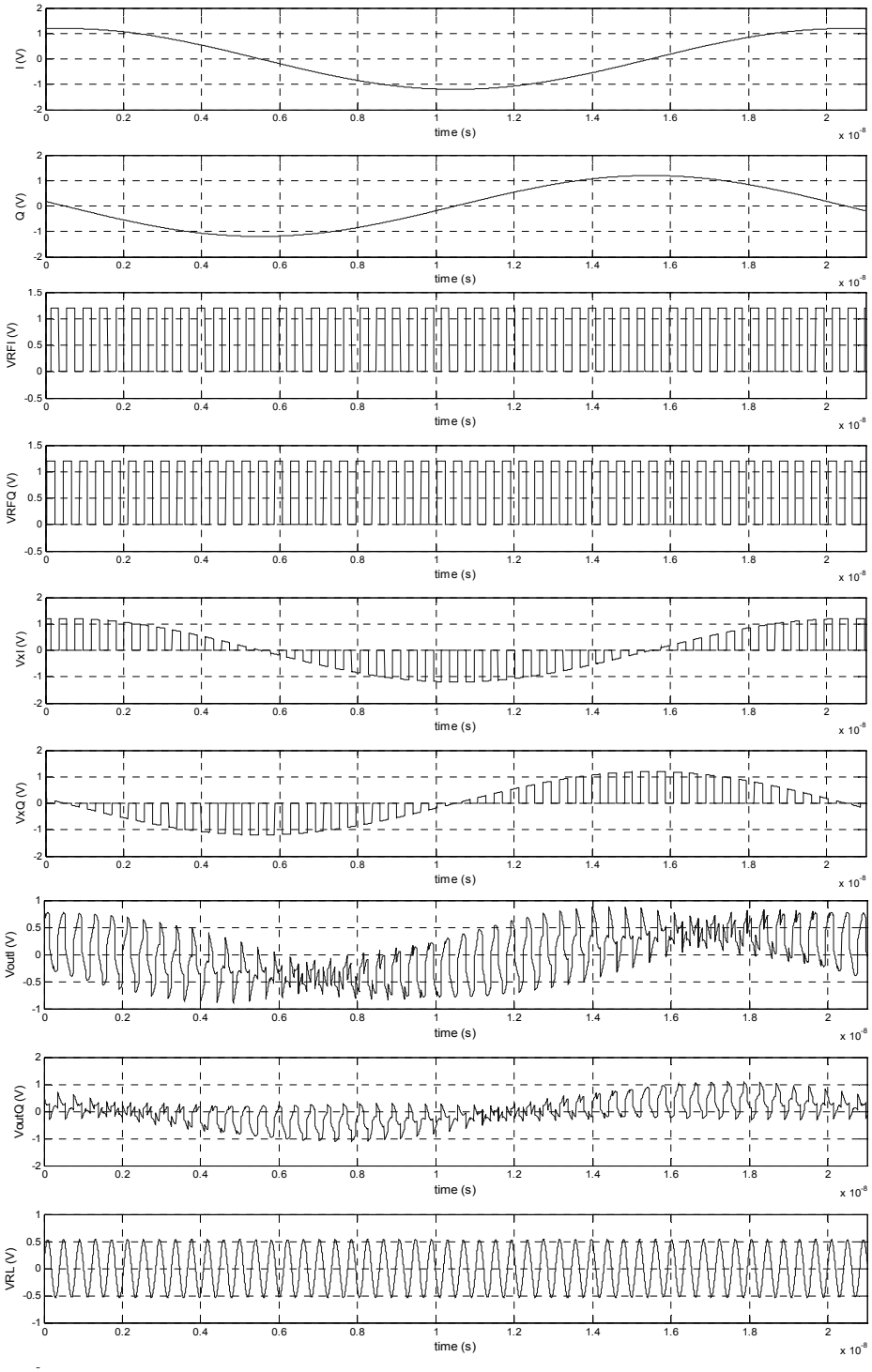

Figure 25 input and output voltages of a quadrature PA using ideal switches

Again, the nodes V_{xI} and V_{xQ} are amplitude modulated RF pulse signals, where its envelope follows respectively I(t) and Q(t). Suppose these I(t) and Q(t) signals are sinusoidal as in Figure 24, then as according to §3.2, the voltage across the load, e.g. the difference between the two output signals should be an RF sinusoidal with constant amplitude. Shown in Figure 25 are the input and output voltages of the described quadrature power amplifier using ideal switches.

The signals at the nodes V_{xI} and V_{xQ} show an RF signal multiplied with the voltage supply and are similar to the same nodes for a single end, quadrature PA.
The voltages V_{outI} and V_{outQ} show an unusual shape. This can be explained by the second LC network seen by each output. Using a resistor, any cross talk between each side is also modeled. This cross-talk can be seen at nodes V_{outI} and V_{outQ}: the waveforms exhibit some higher order harmonic caused by the LC network of the other side of the bridge. Furthermore, both signals are interchangeable depending on which side leads or lags in phase. Since no active device is connected to these nodes, the unusual waveforms at V_{outI} and V_{outQ} are not a problem.
The voltage across the load, V_{outI}-V_{outQ} is as expected a harmonic waveform with constant amplitude.

Shown in Figure 26 is the power spectrum of the output and it shows, as expected, a single sideband suppressed carrier characteristic. The single tone output is indeed shifted up in frequency with a translation equal to the quadrature bandwidth of 50MHz, from the RF frequency 2.4GHz to 2.45Ghz. The maximum magnitude of the output is V_{RL}=576.0mV and is less than the theoretical maximum due to the bandpass characteristic of the LCR filter.

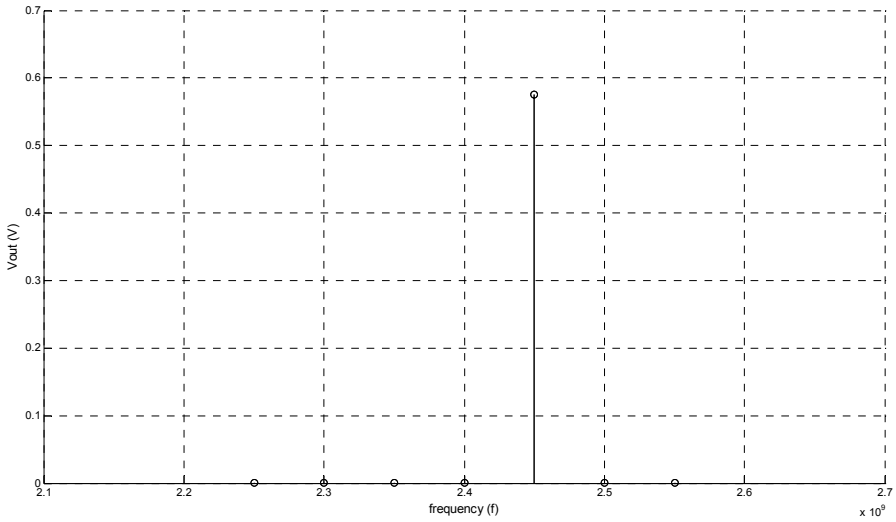

Figure 26 power spectrum of the output of the quadrature PA using ideal switches

3.5. Quadrature PA model with transistors for positive or negative supply

To implement the ideal model as a circuit in real life applications, transistors will have to be used to operate as switches. Using the model with ideal switches as shown in Figure 21, a model with transistors is easily made. Replacing the switches, as in class-D PA, with PMOST and NMOST devices, a single end PA model such as in Figure 27 is obtained.

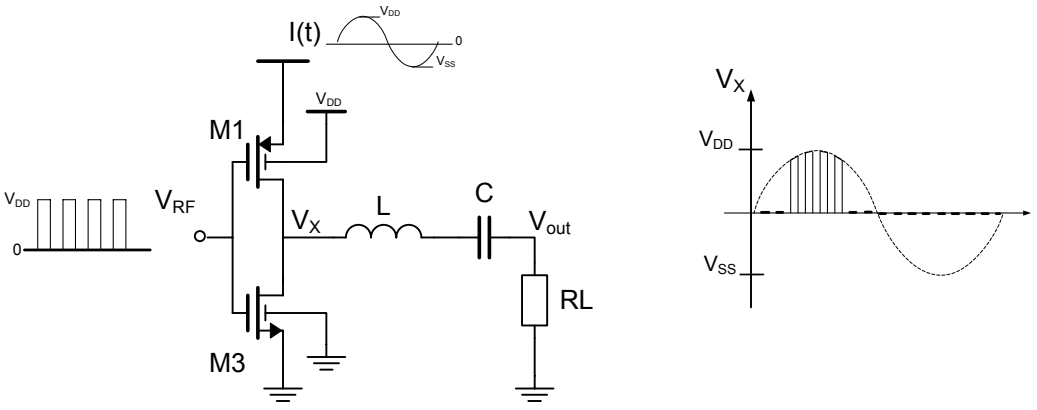

Figure 27 single end quadrature power amplifier class-D operation using transistors

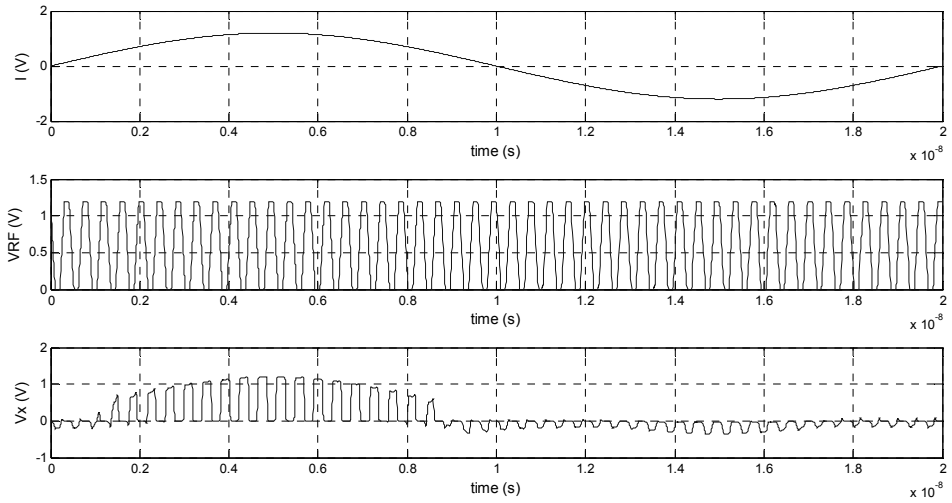

Figure 28 input and output voltages of a single end quadrature PA class-D. For viewing purposes the rise and fall time of the RF signal is set to 100ps.

Running the single end quadrature PA in class-D operation with transistors, using the same signal set as in §3.4, the waveforms of Figure 28 are found. Two main problems, using this topology are evident. First, the output doesn't follow the input for the total positive half, as gaps are shown at t=0..1ns and t=9ns..10ns. Secondly, the circuit is not suitable for a negative voltage supply. Since I(t) can be any arbitrary voltage level and either positive or negative, the circuit needs to able to handle these voltages.

The first problem is caused by the low source voltage of the PMOST. Since the quadrature signal I(t) can have arbitrary voltage levels between V_{DD} and V_{SS}, the situation can occur that the gate-source voltage rises above the threshold voltage, $V_{THPMOST}$ of the PMOST device. This is the case for when the supply voltage I(t) is lower than $V_{THPMOST}$, forcing the device to turn off. The result is that the gate source voltage of the transistor will be too low to switch the transistor on and the transistor won't conduct current.
This can be solved by placing an NMOST device parallel and drive this with an inverted gate signal. The result is transmission gate style switch; for an I(t) with a high voltage level the PMOST is conducting, while the NMOST is turned off. And vice versa: for an I(t) with a low voltage level the NMOST is conducted, while the PMOST is turned off. The result is that the output at node V_x is now a supply modulated RF pulse signal modulated which envelope tracks the total positive range of I(t) continuously.
Figure 29 shows this concept and Figure 30 shows simulations plots of the model. For convenience the LCR filter is omitted.

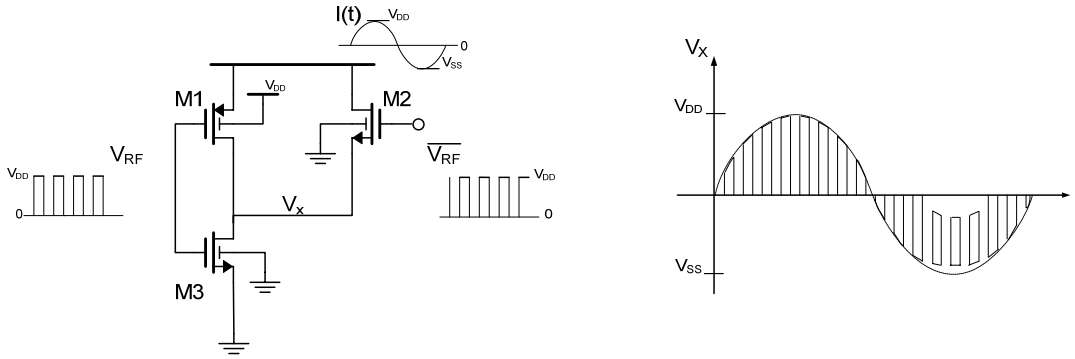

Figure 29 configuration for positive signed I(t)

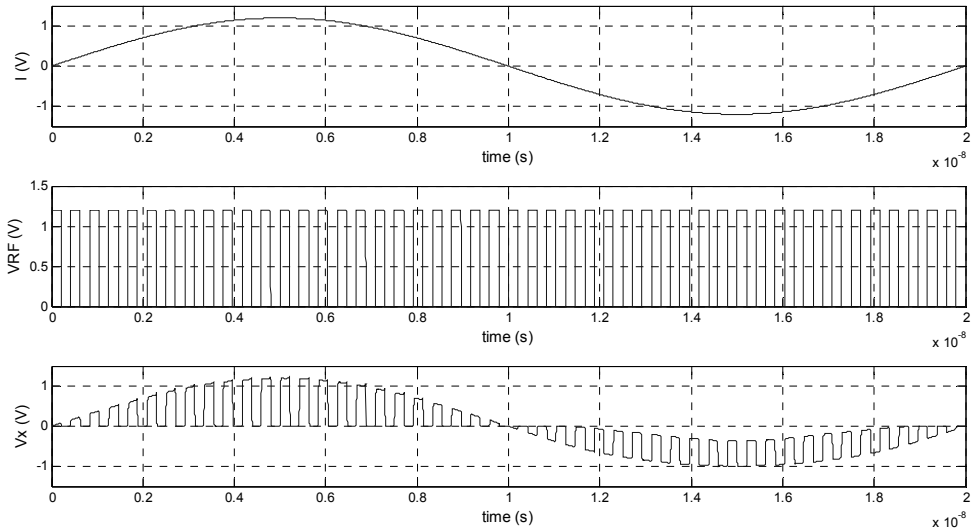

Figure 30 input and output voltages for single end quadrature PA configured for positive signed I(t)

The second problem is due to the fact that the circuit is designed for voltage levels between zero (ground) and the maximum positive voltage V_{DD}. This can also be seen in Figure 29 and Figure 30. If I(t) is signed positive the output is a perfectly modulated RF signal, but if negative signed, the output fails to; transistor M3 is not able to switch to ground and the pair M1 & M2 is not able to fully switch to V_{SS}. This is because as I(t) drops, a back gate diode is biased forward. Shown in Figure 31 is the cross section of a transistor layout of Figure 29. If I(t) drops to V_{SS} a forward biased PN junction is created between bulk and source or drain for transistors M3 and M2. This causes non proper operation of these transistors, resulting in the gaps shown in the waveform at node V_X for a negative signed I(t).

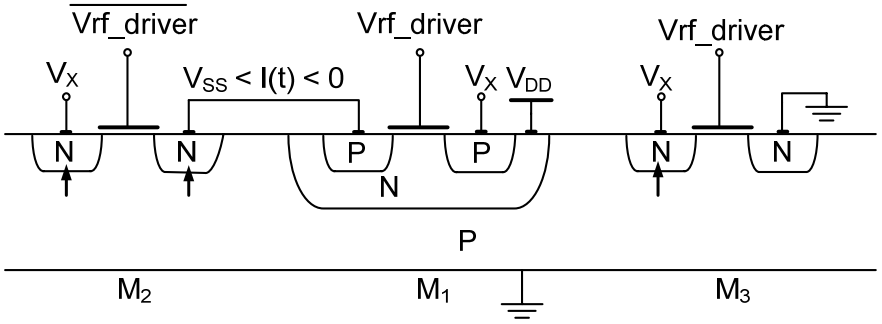

Figure 31 cross section of circuit lay out configured for positive but operating with negative I(t). Forward biased PN junctions are denoted with an arrow

These back gate diodes can be avoided by properly connecting the bulk of the NMOST devices to the lowest potential in the system i.e. V_{SS}=-1.2V. However, a third effect is evident; as I(t) is approaches V_{SS}, while V_{RF_driver} is V_{DD}, the gate source voltage exceeds the maximum allowable voltage and device breakdown will occur. Thus, the configuration of Figure 29 operates only correctly if I(t) is signed positive.

To accommodate negative voltage the whole circuit and driver signal have to be redefined for voltages for between zero (ground) and the minimal negative voltage V_{SS} while I(t) is negative. To avoid voltage breakdown, the RF signal has to be redefined as well. While, for correct and practical continuous operation it is necessary that the supply line is the same node for both positive and negative I(t).

Using the model of Figure 29, a model operating with negative signed I(t) is easily configured. First, the lowest potential will be V_{SS} and the highest zero (ground). The RF driving signal will have to switch between these levels to drive any transistor. If the drive signal is zero, the transmission gate will now pass I(t), with I(t) ranging from V_{SS} to zero. If the drive signal is V_{SS}, the output should be zero. This is done by replacing the NMOST switch with a PMOST. The last step is to define the bulk of all devices to the lowest potential for NMOST devices and to the highest potential for PMOST devices, which would be ground for the case of negative signed input. The result can be found in Figure 32.

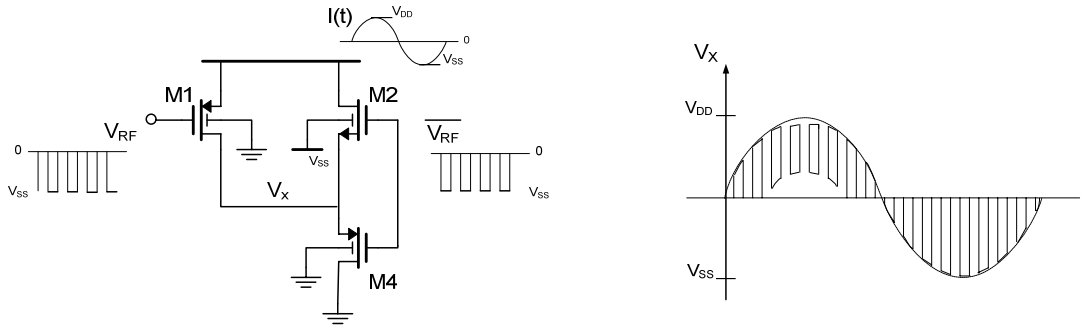

Figure 32 configuration for negative signed I(t)

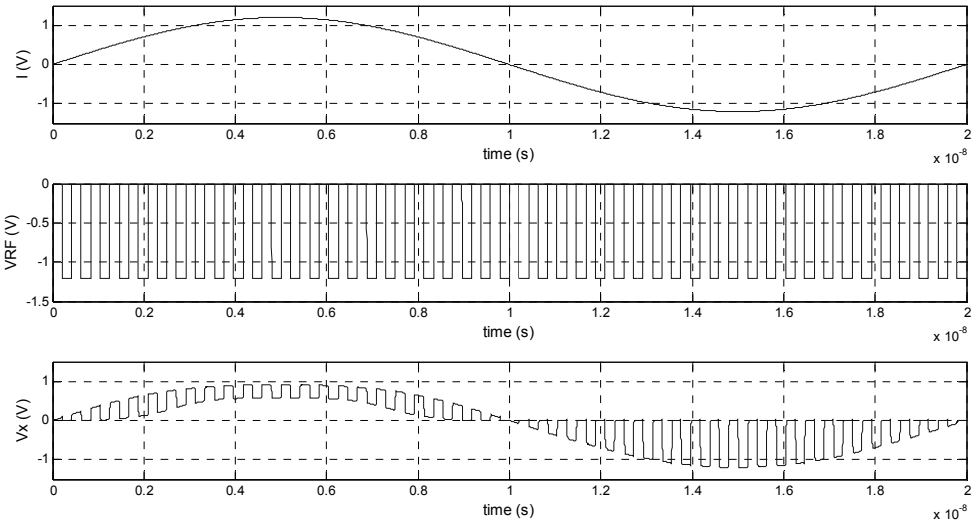

Figure 33 input and output voltages for single end quadrature PA configured for negative signed I(t)

Simulation plots are shown in Figure 33. It can be seen that the circuit is operating correctly for a negative signed I(t), as it shows that the output at node V_X is indeed a supply modulated RF pulse signal, which envelope tracks the negative I(t). But it shows gaps in the waveform at node V_X for positive signed I(t). Again, but this time as I(t) rises, back gate diodes are created in transistor M4 and M1. This can be illustrated in a cross section of the structure of the model in Figure 34. To avoid these back gate diodes, the bulk of the PMOST, M1 and M4 will have to be connected to the highest potential V_{DD}. But, also as the RF input switches between V_{SS} and ground, the configuration of Figure 32 gives rise to voltage breakdown of the devices when I(t) signed positive. With other words, this configuration operates correctly only and only then when I(t) is signed negative.

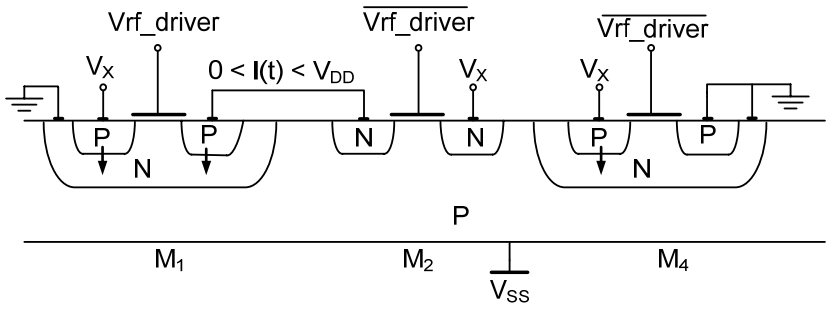

Figure 34 cross section of circuit lay out configured for negative but operating with positive I(t). Forward biased PN junctions are denoted with an arrow

Figure 29 and Figure 32 show an implementation for transistors for class-D style architecture for a switching power amplifier. Its voltage supply line can be used for

amplitude modulation using a continuous signal. For positive signed supply voltages, the model of Figure 29 can be used and for negative signed supply voltages the model of Figure 32, since neither model is suitable for both positive and negative signed supply voltages. Furthermore both models need a different RF signal to drive the switch mode transistors. Though these models do operate correctly, it would be costly, components- and power-wise to implement an architecture using two models, with each its own operation conditions. If bridged, creating a quadrature power amplifier, eight of these single ended PA in four configurations would be needed to operate at all voltage combinations. This would require a huge amount of components, wiring and logic to switch the proper architecture for specific voltage conditions. A single architecture capable to handle both positive and negative supply voltages would need only two single ended PA, one for each side of the bridge. This would limit the use of wires, components and logic, thus reducing costs and power.

3.6. Quadrature PA model for both positive and negative supply

The models of Figure 29 and Figure 32 in §3.5 can operate properly, but only for either a positive or negative supply voltage. However, a single architecture that is able to handle both positive and negative supply voltages is preferred for simplicity. To do this, the circuits of Figure 29 and Figure 32 can be combined as seen in Figure 35. The result is a switching modulating amplifier configured for modulation signals between V_{DD} and V_{SS}. The driving RF signal is now a function of the sign of the quadrature signal I(t). For a positive signed I(t), the RF signal switches between zero and V_{DD}, for negative signed I(t) between V_{SS} and zero. Figure 35 shows the output at node V_X and shows a modulated pulse signal for the full range of I(t). An LCR network, not shown in Figure 35, will pass the fundamental tone and the result at the output is an amplitude modulated sinusoid waveform.

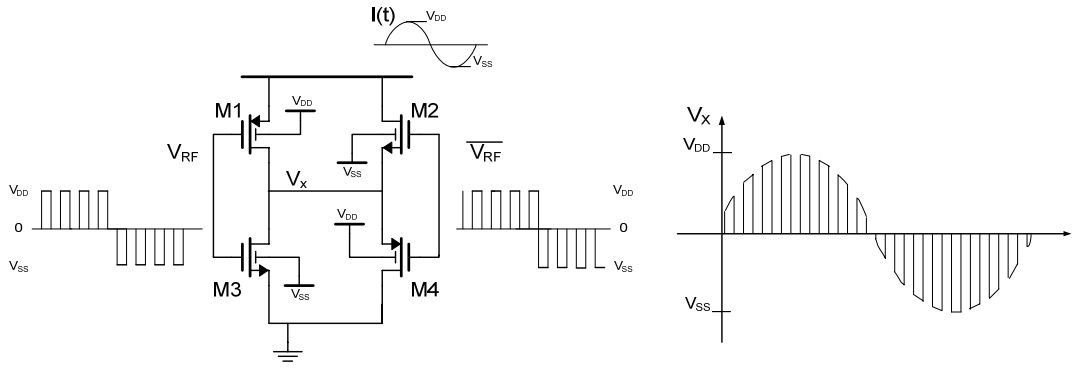

Figure 35 configuration for both positive and negative I(t)

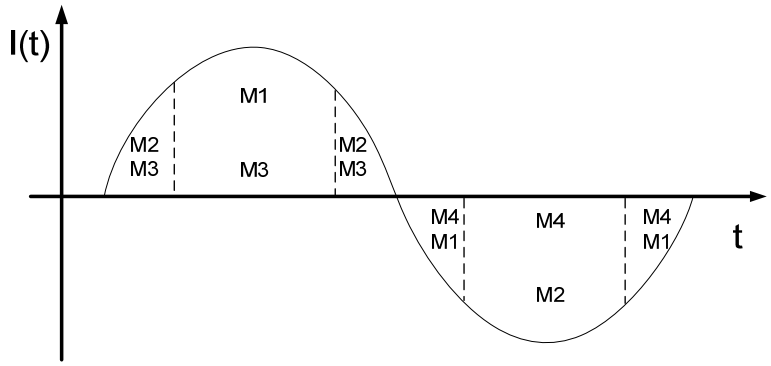

Figure 36 operating regions of the transistors as function of I(t)

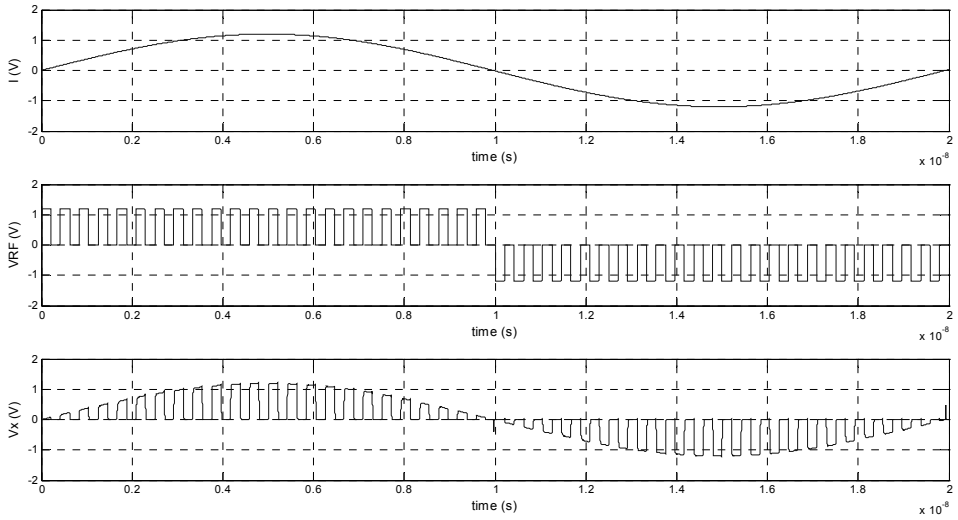

Figure 37 input and output voltages for single end quadrature PA configured for positive and negative signed I(t)

Figure 36 summarizes schematically which transistor pair is operating as function of I(t). For a positive signed I(t), transistor pair M1 and M3, or M2 and M3 are operating depending on the gate source voltages of the transmission gate pair M1 and M2. For a negative signed, similar operation can be found for transistor pair M1 & M4 and M2 & M4.

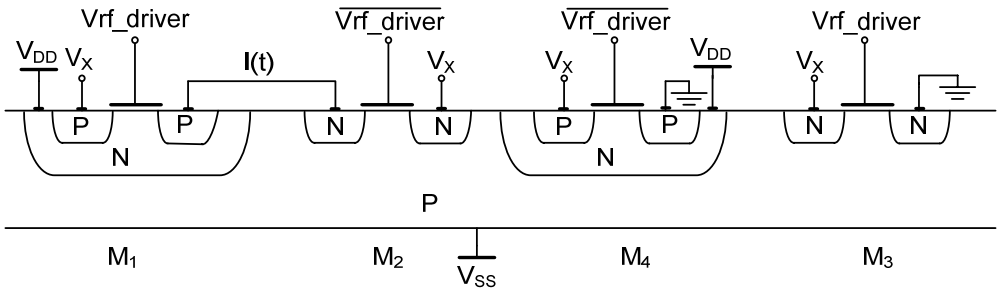

Figure 38 cross section of circuit layout configured for both positive and negative I(t)

The driving RF signal has to be a function of the supply voltage I(t) i.e. it has to switch between zero (ground) and V_{DD} or V_{SS} dependent of I(t). While a full swing signal, from V_{DD} to V_{SS} would reduce the need for some kind of logic to generate such dependent RF signal, gate oxide breakdown would be unavoidable. Shown in Figure 38 is the cross section of the transistor lay out as would be the case for the model of Figure 35. Suppose, the RF signal is $V_{RF}=V_{DD}=1.2V$ while $I(t)=V_{SS}= -1.2V$, the gate source and gate drain voltages of devices M_1 and M_2 is $V_{GS}=V_{DS}=2.4V$. This exceeds the maximum allowable breakdown of $V_{breakdown}=1.2V$ for the used transistors and as stated, would result in gate oxide breakdown.

To avoid this, the use of thick gate oxide devices can be employed. Though, such thick gate oxides devices are capable of handling higher breakdown voltages, these devices also tend to be slower due to thicker gate oxide and the larger minimal length of these devices. Since the PA has to operate at RF frequencies, it is preferable to avoid the use of thick gate oxide devices in the signal path. Therefore, using a RF signal dependent of I(t) is a necessity to proper drive the PA.

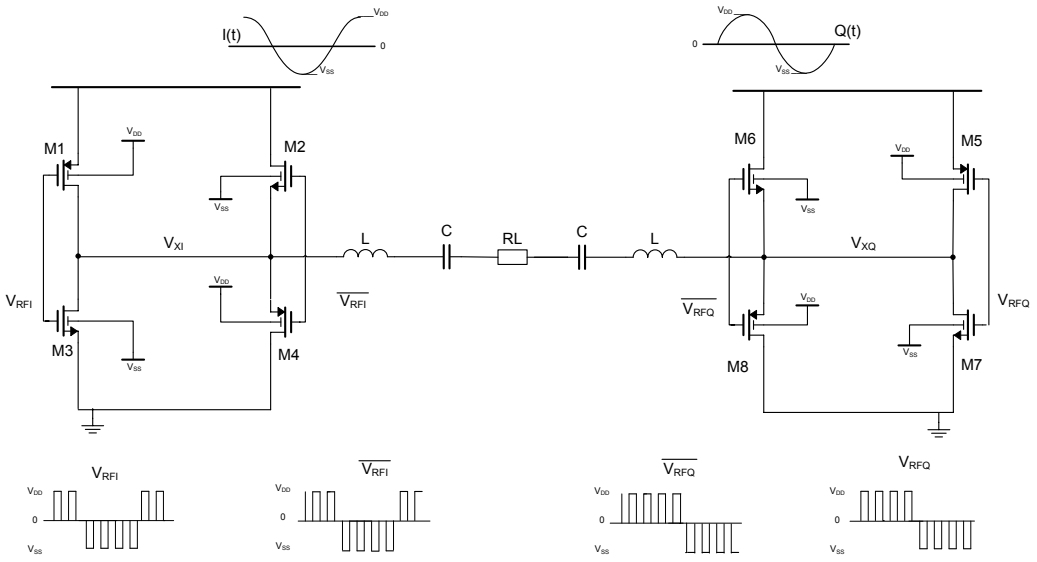

Figure 39 quadrature power amplifier

Placing two of these quadrature modulated amplifiers in bridge, gives the circuit of Figure 39. Just as the model with switches each side is modulated with either an I(t) or a Q(t) signal. Also, each side is driven with a RF hard switching signal with 90° difference in phase. However an additional RF signal is needed as shown in Figure 35. The result and typical waveforms can be found in Figure 39.

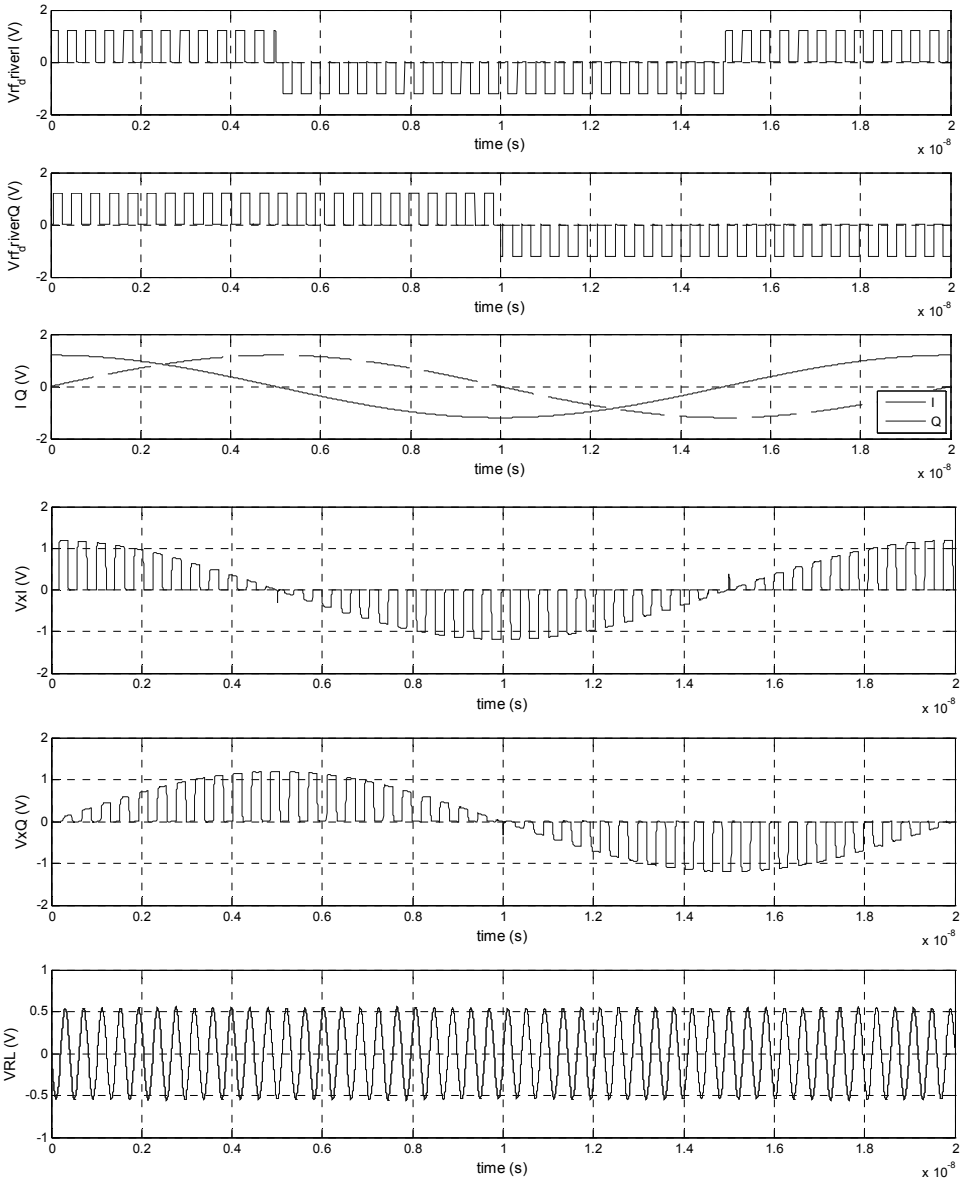

Figure 40 waveforms for a quadrature PA

Shown in Figure 40, the waveform for the model with transistors are similar to that of the model with switches. As described above, the RF driver signals are a function

of the sign of the quadrature signals I(t) and Q(t). As the sign is positive, the RF signal switches between zero and V_{DD} and if negative, the RF signal switches between V_{SS} and zero.
For a quadrature signal set of sinusoidal waveforms, it was shown that the output across the load is a constant amplitude RF sinus waveform. The output of the quadrature PA with transistors correspond thus with the output of the quadrature PA modeled with ideal switches.

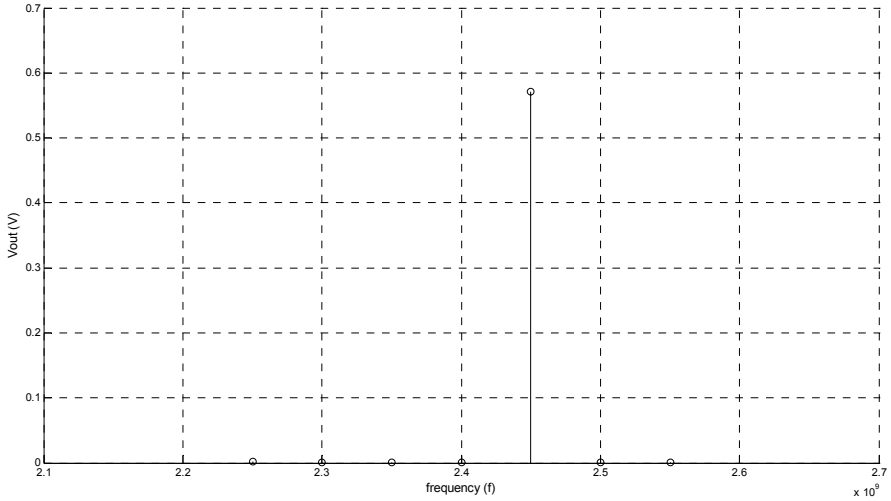

Figure 41 spectrum power of the voltage across the load of quadrature PA

Figure 41 shows the spectrum of the voltage across the load of the bridged quad PA and shows a single tone output, which is shifted up in frequency. This single sideband suppressed carrier characteristic is similar to the output for the model with switches.

3.7. Quadrature PA model with transistors for positive and negative supply voltages and bulk switches

Using the transmission gate topology, the use of voltage supply modulation by I(t) and Q(t), ranging from V_{DD} to V_{SS} has been made possible. As shown in §3.5, the PMOST device conducts a “high” voltage and the NMOST for a “low” voltage, assuming the proper gate voltages.
This principle can be described using the on-resistance of the switch. If a transistor is used in switch mode, it operates in deep triode region, i.e. $V_{DS} << 2(V_{GS}-V_{TH})$. In that case, the drain current is a linear function of the drain source voltage and not independent as is the case for the saturation region as found in linear mode power amplifiers.

$$I_D = \mu C_{ox} \frac{W}{L}(V_{GS} - V_{th})V_{DS} \qquad (14)$$

In other words, there is a linear relation between the voltage and current: the transistor acts as a linear resistor, which can be controlled by the overdrive voltage (V_{GS}-V_{TH}). If a transistor acting as switch is on i.e. it conducts current, there will be a finite on-resistance equal to:

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{th})} \qquad (15)$$

If the switch is off, i.e. it conducts no current; there will be an infinite resistance.
For a transmission gate, as shown in Figure 42, the on-resistance for a PMOST is infinite for a high input voltage and finite for a low input voltage and for a NMOST, vice versa. Ideally the result is an overall constant finite resistance independent of the input signal.

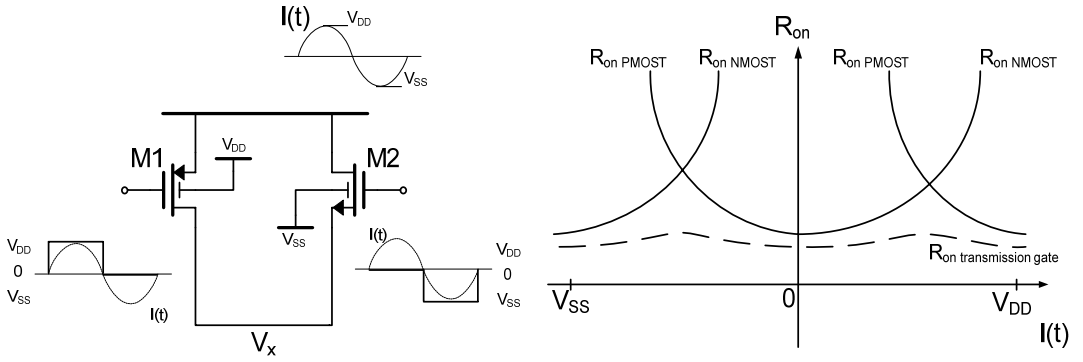

Figure 42 on-resistance as for the transmission gate style single end quadrature PA

However, in practice this overall on-resistance of the transmission gate is not constant. There is a peak at the transition between PMOST and NMOST operation. The peak to average ratio can be sufficient to be noticed at the output. At these transitions the on-resistance is increased, dissipating power and degrading the overall power efficiency.

This effect is further increased by the body effect. In a quadrature PA as shown in Figure 39, the bulk of the NMOST is connected to V_{SS} and the bulk of the PMOST is connected to V_{DD}. Assume a positive signed I(t), then the potential at the bulk of the NMOST devices is lower than at the source. For a negative signed I(t), the potential at the bulk of the PMOST is higher than at the source. Both situations

increases the body effect of NMOST and PMOST. This results in an increase of the threshold voltage. Simulations show that the threshold voltage is increased from $V_{thNMOST}$=0.51V to $V_{thNMOST}$=0.64V for the used NMOST model and $V_{thPMOST}$= -0.28V to $V_{thPMOST}$= -0.43V for the used PMOST models. From *(15)* it is clear that in this case, the on-resistance will increase as well: in Figure 42 the $R_{onNMOST}$ for positive I(t) and the $R_{onPMOST}$ for negative I(t) will move up, resulting in a higher peak of the overall on-resistance at the transition between PMOST and NMOST operation.

To minimize this effect the bulk can be switched to accommodate the proper bulk voltage for either positive or negative signed I(t). This idea is schematically illustrated in Figure 43, if I(t) is signed positive, the PMOST bulk is connected to V_{DD} and the NMOST to ground, if I(t) signed negative, the PMOST bulk is connected to ground and the NMOST bulk to V_{SS}. Thus, the bulk of the devices are always connected to the highest and lowest voltages that are currently present in the system.

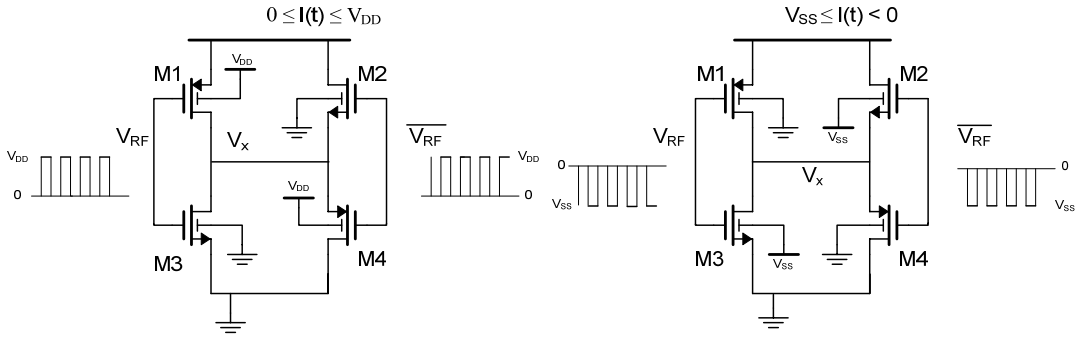

Figure 43 single end quadrature PA configurations with switching bulk voltages to reduce the on-resistance. Left situation is configured for positive signed I(t), right situation for negative signed I(t).

The resulting on-resistance is plotted in Figure 44. As comparison is the on-resistance for both with and without the switched bulk voltages plotted. It can be seen that for positive signed I(t) the Ron of the NMOST decreases and for negative signed I(t) the Ron of the PMOST decreases. The result is a lower peak to average ratio in the on-resistance for the total range of the envelope signal.

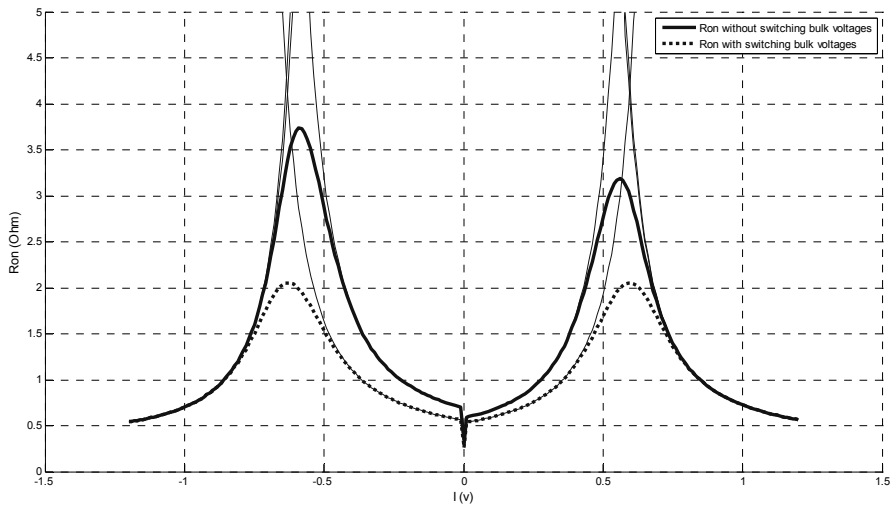

Figure 44 on-resistance of a single end quadrature PA for with and without switched bulk voltages

Though in absolute terms, the value of Ron that is minimized is not that much when modeled with a 50Ω load, but in practical situation this could be a lot. As suggested in §3.4, a practical implementation would require a smaller load resistance and the use of impedance transformation. In that case, the decrease of Ron using switched bulk voltages with approximate 40% using shown in Figure 44 could be a huge fraction of the used load resistance.

The bulk switches can be realized using the topology as shown in Figure 45. For switching between ground and V_{DD} a PMOST and NMOST as a digital inverter can be used. For switching between V_{SS} and ground a PMOST and NMOST as a inverted digital inverter can be used. The gates of the switches is driven by signal SI(t), which is equal to V_{DD} when I(t) is signed negative and V_{SS} when I(t) is signed positive. The result is that the bulk is switched to either V_{DD}, ground or V_{SS} at the proper moment depending on the sign of I(t).

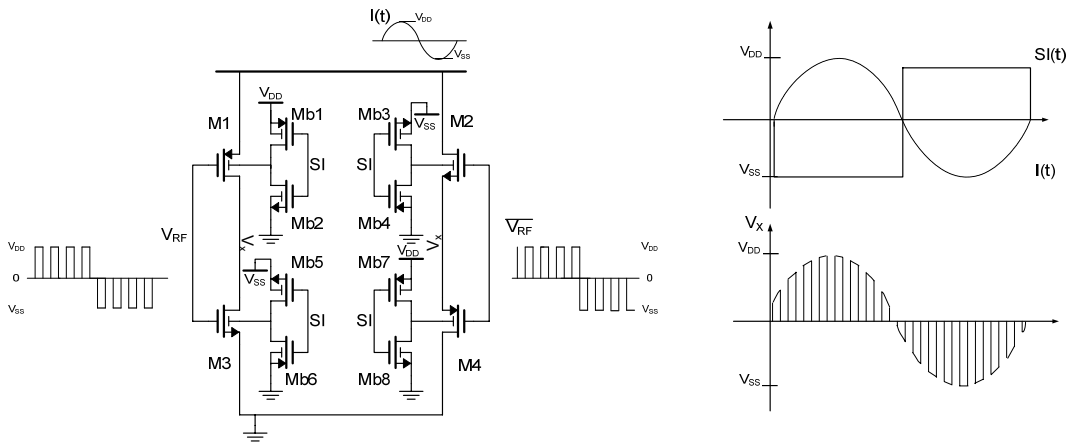

Figure 45 single end quadrature PA using bulk switches

Since a full swing signal as SI(t), ranging from V_{DD} to V_{SS}, is used to drive these bulkswitches, the transistors will exceed the maximum gate-source and gate-drain voltage level of 1.2V set by the used technology. The usage of thick gate oxide devices that can handle higher voltages will be necessary; the downside is that these devices are slower due to the thicker oxide. But, these bulk switches are not a part of the RF signal path and the driving signal SI(t) is a function of I(t) and thus a relatively low frequent signal. Thus, speed is not a critical issue.

Shown in Figure 46 is the structure cross section of a single end quadrature PA. If the transistors that make up the bulk switches are realized as thick gate oxide devices as said, no gate oxide breakdown occurs. However, to isolate the bulk so it is able to handle two different voltages, a triple well technology has to be used. For example, consider device M_2 and a positive signed I(t). In that case, the bulk of M_2 will be connected to ground. Without the deep N-well, there would be a violation since the P-substrate is connected to V_{SS}. Now, consequently the substrate can be connected to ground, but in that case the problem occurs again if I(t) is signed negative, connecting the bulk of M2 to V_{SS}. Thus a triple well provides any necessary isolation between the bulk of the devices and the substrate.
Furthermore, just as for the quadrature PA without bulk switches, if the driving RF signal is a function of the sign of I(t), no back gate diodes will be turned on.

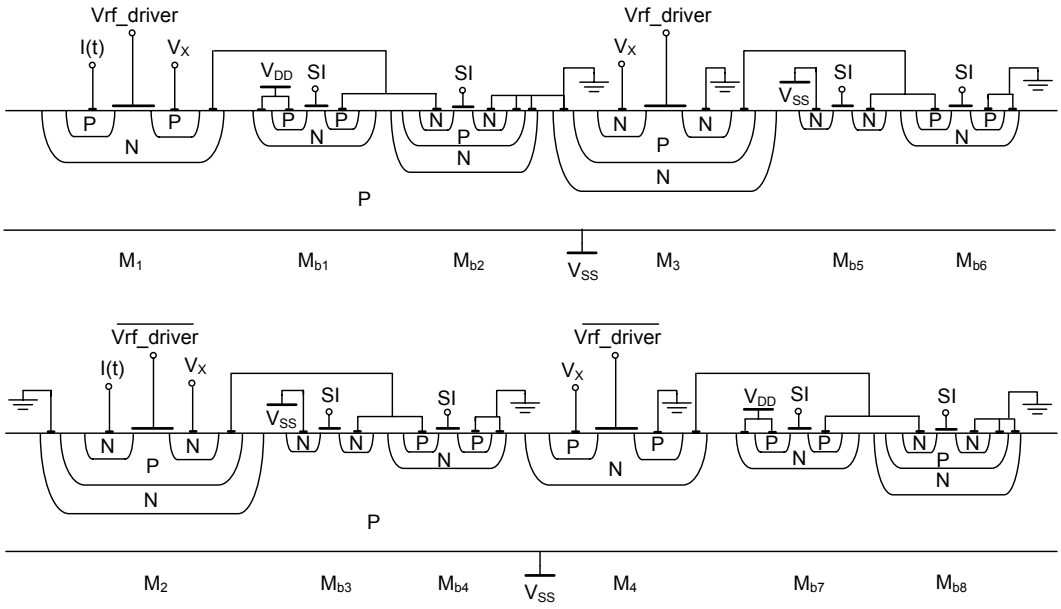

Figure 46 cross section of transistor lay out of a single end quadrature PA with bulk switches

An alternative to smoothen the on-resistance is to increase the overdrive voltage in equation *(15)*. This can be achieved by driving the main resistors M1-M4 in Figure 39 with a gate signal of V_{DD} to V_{SS}. However, this will need thick gate oxide devices in the RF signal path. As stated before, it is favorable to avoid this option, because thick gate oxide devices are slower compared to conventional gate oxide dimensioned devices. Especially should this option be avoided since in this case these slower transistors will be placed in the RF signal path.

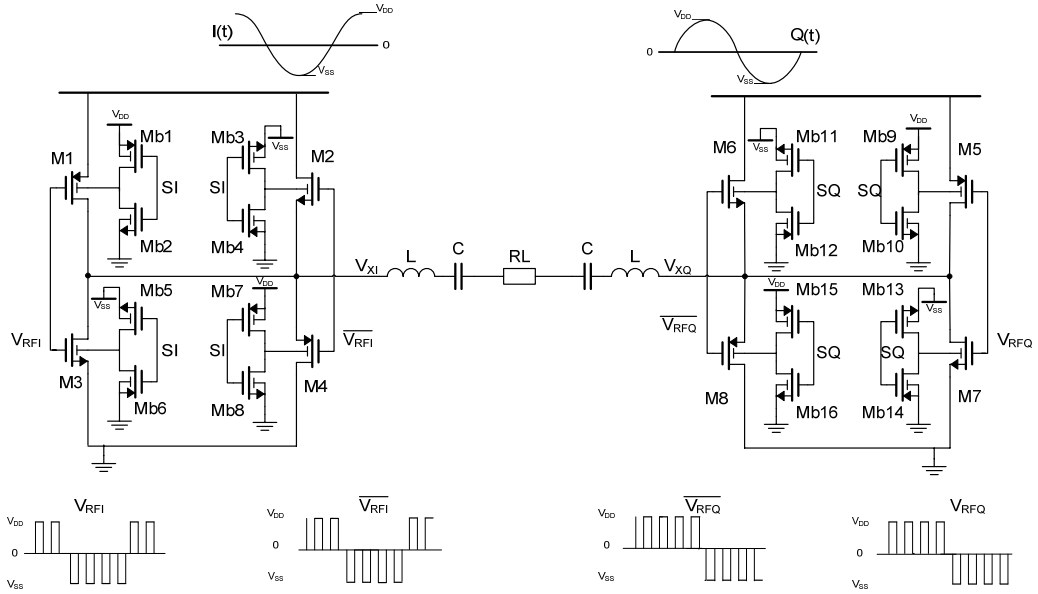

Figure 47 quadrature power amplifier

Figure 47 shows, the quadrature power amplifier in bridge mode, but with the added switches for the bulk. Simulation waveforms are shown in Figure 48. The power spectrum of the output voltage across the load is shown in Figure 49

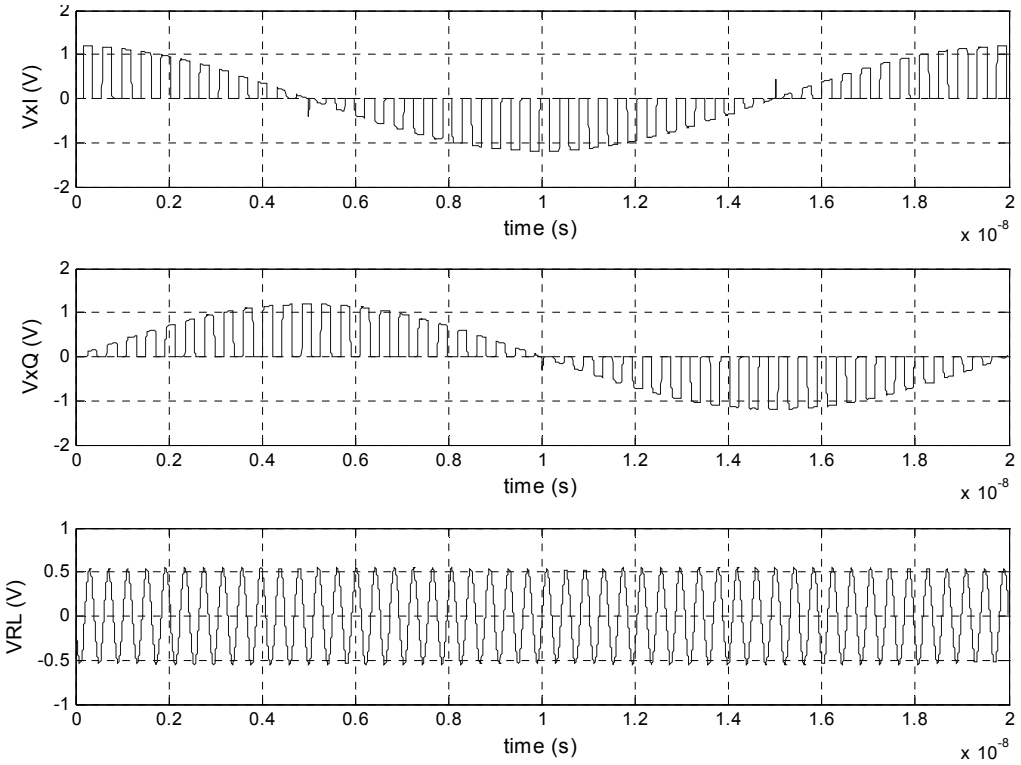

Figure 48 waveforms for a quadrature PA with switched bulk voltages

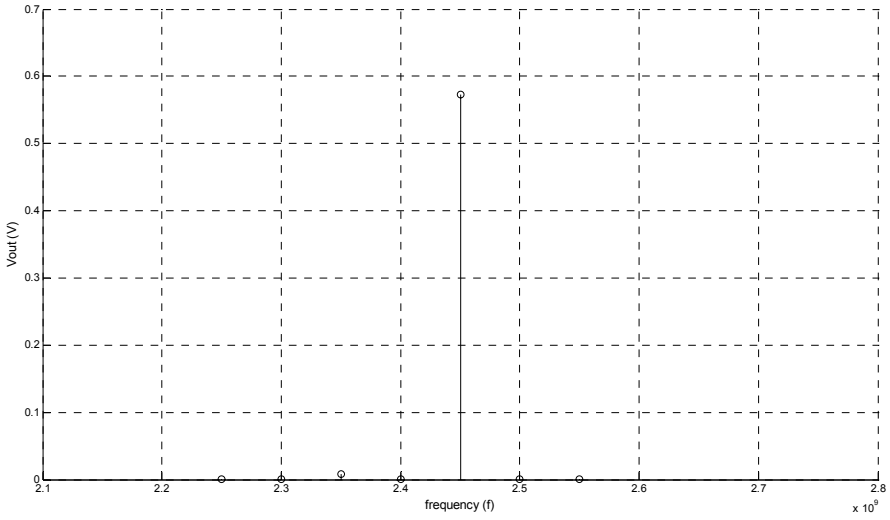

Figure 49 spectrum power of the voltage across the load of quadrature PA with switched bulk voltages

Essentially, the waveforms show the same result as the model with switches and the model without the bulk switches. The set of switches multiply the RF driving signal ($V_{rf\_driverI}$ and $V_{rf\_driverQ}$) with the quadrature signals I(t) and Q(t) for the total range of V_{DD} to V_{SS} (nodes V_{XI} and V_{XQ}). An LC-tank filters out the fundamental and the outputs of each side are subtracted across the load R_L resulting in a constant envelope sinusoid (V_{RL}) if the quadrature signals are sinusoidal.
Again, the power spectrum shows a single peak, shifted from the RF-frequency with the quadrature bandwidth, in this case 50MHz, to 2.45GHz.

model	V_{out} (mV)
using ideal switches	576.0
without bulkswitches	571.8
with bulkswitches	573.5

Table 4 spectrum magnitude for each model using the same simulation

Table 4 shows the magnitude of this peak for the different models. Theoretically, the model using ideal switches exhibits neglectable losses due to on-resistance and the model without bulk switches the most. The model with bulk switches is somewhere in between and this shows in the magnitude. Though the differences are small, it is evident that the model with the bulk switches approximates the value of the model using switches better. As said, the differences will be more evident if the on-resistance is a noticeable fraction of the load resistance i.e. a smaller load resistance is used.

3.8. Losses and sizing

Due to capacitances, resistive channel and continuous voltage and direct path currents the transistor is not an ideal switch. By using transistors as switches for the quadrature PA model without bulkswitches, as in Figure 39 and with bulkswitches as in Figure 47, one introduces degradation of performance and efficiency.

For all switched mode power amplifiers, three main mechanisms of losses can be found: conduction losses, switching losses and losses due to direct path currents. These will be discussed in the following paragraphs. Since these mechanisms are a function of transistor dimensions, sizing of the devices will be crucial if power efficiency is considered. The last paragraph will deal with proper sizing to achieve minimal losses, while maintaining the proper operation.

3.8.1 Conduction losses

The losses found as power dissipation associated with resistances in semiconductor devices and passive components are called conduction losses. In transistors, conduction losses are present in both dynamic and static operation and the channel resistance of a transistor is dependent of gate source voltage
The on-resistance has been described in §3.7 as *(15)*. However, this equation is valid for the assumption that the drain current is linear for small $V_{DS.}$ In practice this is not the case. As a result the on-resistance is non linear and changes even during the on-state. This can also be seen in Figure 42. Including this variation the on-resistance can be described with

$$R_{on} = \frac{V_{DS}}{I_D(V_{DS})} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th}) - \frac{V_{DS}}{2}} \qquad (16)$$

while:

$$I_D(V_{DS}) = \mu C_{ox}\frac{W}{L}(V_{GS} - V_{th}) - \frac{V_{DS}^2}{2} \qquad (17)$$

Note that, for V_{DS}=0, this equation reduces to *(15)* in §3.7, which resulted from the assumption that V_{DS} is small and I_D is constant.

The on-resistance decreases with the width of the transistor but increases for reduced supply voltages. The first is logical and the second makes sense because if the overdrive voltage of the transistor is smaller, the transistor conducts less current.

Conduction loss in passive components is dependent of parasitic resistance in metal wires and the Q-factor. For an inductor: $Q=\omega L/R_s$, a capacitor: $Q=1/\omega R_s C$ with R_s denoting the series resistance. For capacitors the series resistance is usually quite small and can be neglected. However for inductors the wires, wound in several turns, may result in a long wire and thus a more apparent series resistance is present. This series resistance is frequency dependent due to the skin effect. As the frequency increases, the electrons tend to move more at the surface of the wire than at its core. This reduces the effective conduction area and increases the conduction resistance.
It is therefore desirable to keep the inductor small, to limit the size of the series resistance and thus the conduction losses.

Consider the single end quadrature power amplifier without bulkswitches of Figure 35, if both parallel pairs M1-M2 and M3-M4 are replaced by an equivalent ideal switch and on resistance, the circuit Figure 50 is obtained. If the losses are substantial, voltage division takes place between the load R_L and the transistor on-resistance and the inductance series resistance. The result is a deformation of the square wave signal and a reduced output voltage swing, thus certain power is dissipated due to conduction losses.

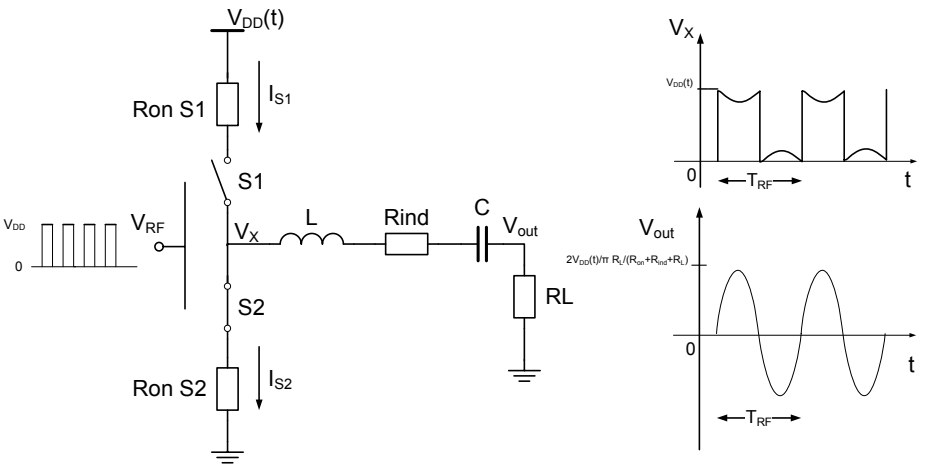

Figure 50 single end quadrature PA model for conduction losses with typical voltage waveforms

3.8.2 Switching losses

Energy losses associated with charging and discharging of parasitic capacitances of a transistor are called switching losses. This energy loss occurs at each discharging with each period of the signal frequency and is therefore frequency dependent.

It can be shown [18] that the switching losses can be expressed as:

$$P_{SW} = (C_G + C_D)V_{DD}{}^2(t)\,f \tag{18}$$

With C_G and C_D respectively the parasitic gate and drain capacitance of the transistor. This result shows that switching losses increase with increasing parasitic capacitances. These capacitances scale with the transistor dimensions. It is therefore favorable to minimize the transistor size to minimize the switching losses. Furthermore, the losses increase with the frequency and are independent of the duty cycle. And lastly, the losses increase with the supply voltage.

3.8.3 Direct path current losses

Ideally the pulse signal that drives the switches has an infinite rise and fall time. In practice these rise and fall times will be finite. For real devices as transistors this means that at certain moments both the PMOST and NMOST will conduct simultaneously. This is shown in Figure 51. This causes a direct current path from

supply to ground and power is dissipated in the on-resistance each period. Losses due to direct path currents are frequency dependent and can therefore also be regarded as switching losses.

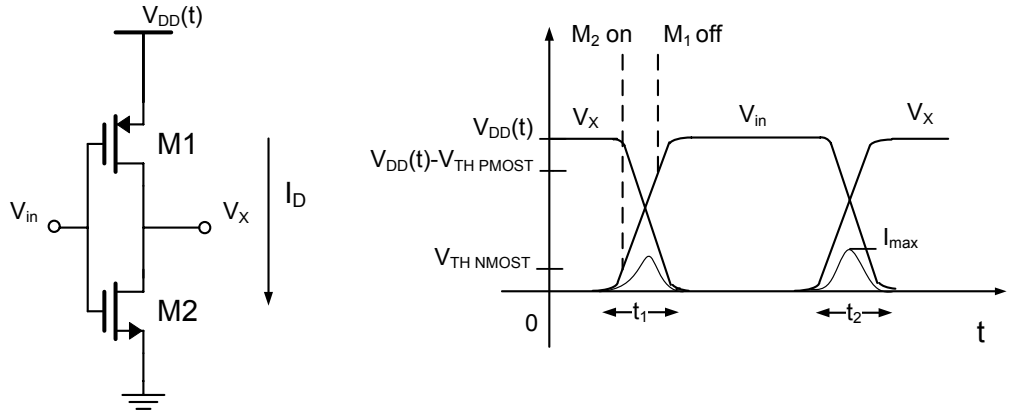

Figure 51 single end quadrature PA model for direct current losses with typical input- and output voltages and current relation

The direct path current I_D reaches its maximum when both transistors are conducting and is dependent on the rise and fall times of the slope, while these are determined by parasitic capacitances of the transistor.

It is shown [18] that the losses due to direct path currents can be expressed as.

$$P_{dp} = \frac{1}{2} V_{DD}(t)(I_D * t_{on1} + I_D * t_{on2})\, f \tag{19}$$

The same as for switching losses, direct path current losses are frequency dependent, but not dependent on the duty cycle. However, it is assumed that the on-period of either switch is longer than the simultaneously on period of both switches. Lastly, the direct path currents losses decrease by decreasing the voltage supply.

3.8.4 Sizing

The previous paragraphs show that losses found in a switching mode power amplifier are dependent of the size of the transistor. However, conduction losses increase with the width of transistors, while switching losses and direct path current losses decreases. This means that there will be a trade-off between the several mechanisms for minimal loss as function of the transistor widths.

Since power amplifiers are measured in terms of power added efficiency, the quadrature PA is dimensioned for best performance in terms of PAE. Using the

circuit of Figure 52, a single end quadrature PA configured for maximum input voltage i.e. $I(t)=V_{DD,}$ the PAE is plotted as function of the width of the NMOST devices for several width of PMOST device. The result is shown in Figure 53.
It should be noted that the PAE noted in this paragraph is not the same as the PAE of the final quadrature PA. For instance, only a single end instead of the full bridge is used, the driver used is an ideal voltage source and the inductor is assumed lossless. Better would be the use of the term drain efficiency or overall efficiency.

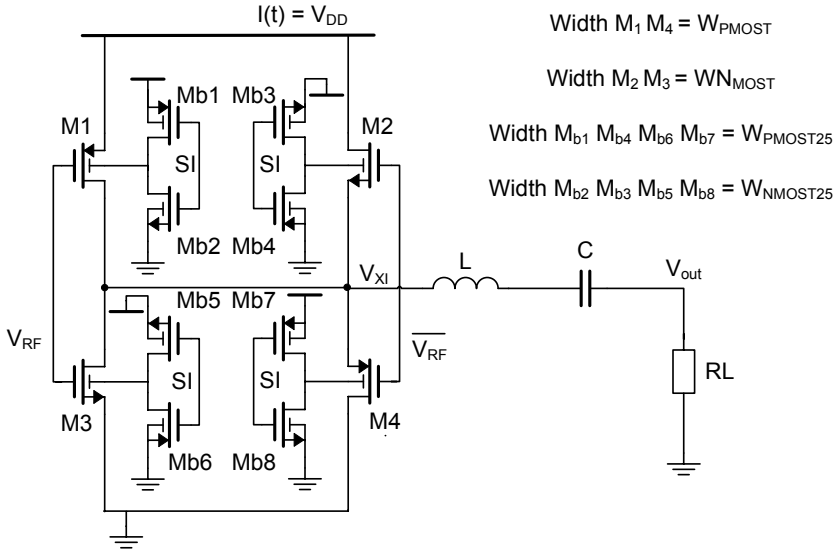

Figure 52 single end quadrature PA for PAE simulation

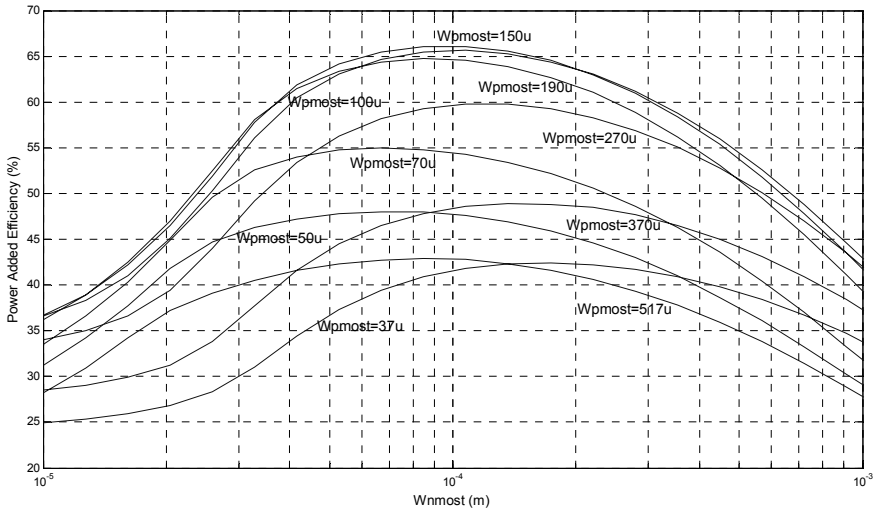

Figure 53 power added efficiency as function of the width of NMOST devices for several PMOST devices

From Figure 53 it can be seen that the PAE is maximized using a NMOST width of W_{nmost}=100µm and a PMOST width of W_{pmost}=150µm while keeping minimum length of L=90nm for both PMOST and NMOST devices.

The resulting voltage output V_x and V_{out} are plotted in Figure 54. It can be seen that the used transistor size increases the on-resistance in such a way that it is noticeable at the output. The result is a heavily attenuated sine with an amplitude of V_{out}=636mV.

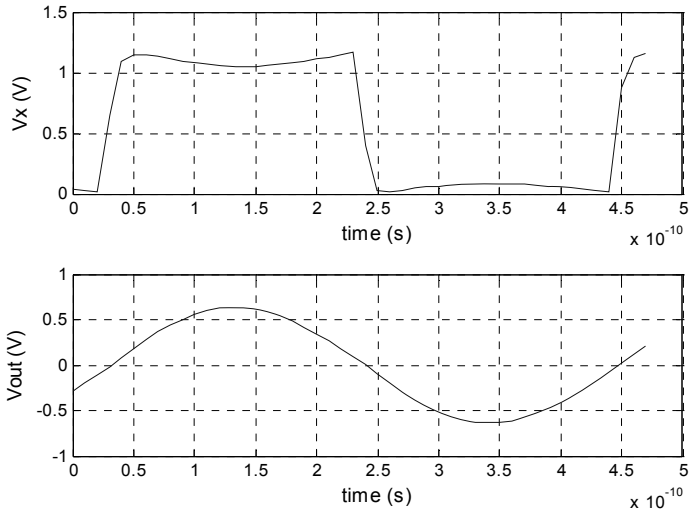

Figure 54 Voltages Vx and Vout for a single end quadrature PA for W_{nmost}=100µm and W_{pmost}=150µm

Such amplitude is 17% different from the theoretical maximum amplitude of V_{outmax}=764mV for a perfect ideal square wave. A trade off between PAE and voltage swing can be made if the application requires a higher voltage swing, In this case however, the goal is maximum power added efficiency.

Now that the transistors in the RF path have been dimensioned, the transistors that make up the bulk switches are left. Again, the size is determined as function of the PAE. The transistors that have to be dimensioned are thick gate oxide devices with a maximum gate voltage of $V_{breakdown}$=2.5V with a minimum length of L_{25}=240nm. Again, the PAE is plotted versus the width of both PMOST and NMOST devices. Two situations have to be examined. First is the situation when I(t) is signed positive. In this case, the PMOST bulk switches are active and connect the bulk of the RF devices to the proper voltage. In this case the NMOST devices are inactive and thus of non importance. Second is the case when I(t) is signed negative and the NMOST bulk switches are active and connect the bulk of the RF devices to the proper voltage. In this case the PMOST devices are inactive and of non-importance.

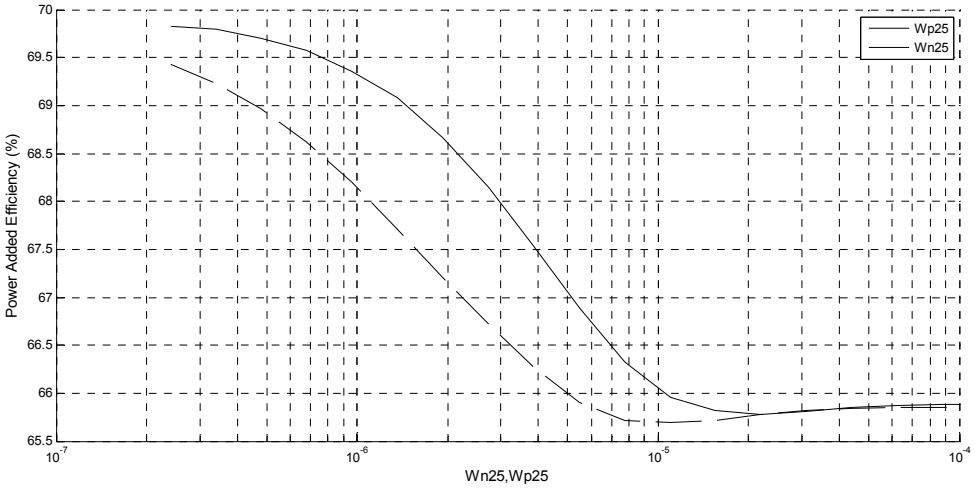

Figure 55 bulk switch width versus PAE

The result shown in Figure 55, shows that, as expected, the transistors for the bulk switches can be dimensioned as small as possible for the highest PAE. Therefore these transistors are set for minimum width, which are set by technology rules, of $W_{PMOST25}$=360nm and $W_{NMOST25}$=360nm, while keeping the length minimal at L_{25}=240nm for both the thick gate oxide PMOST and NMOST devices. Notice that the PAE is increased using these bulk switches. This can be explained by the fact that, using these bulk switches the body effect, consequently the threshold voltage and the on-resistance is minimized, thus reducing any conduction losses.
Table 5 summarizes the dimensions of the transistors for the quadrate PA with and without bulk switches.

device	length (m)	width (m)
NMOST in RF path	90n	100µ
PMOST in RF path	90n	150µ
NMOST as bulk switch	240n	360n
PMOST as bulk switch	240n	360n

Table 5 transistor dimensions for the quadrature PA with and with out bulk switches

3.9. AM-PM Distortion

For conventional polar amplifiers AM-PM conversion, also called feed through is an issue as stated in §2.5.1. This feed through effect results from the parasitic capacitance of the active device between gate and drain. When the drain voltage

drops below a certain level, the RF-driving signal leaks to the drain through this gate drain capacitance. This causes amplitude and phase distortions at the drain, limiting the performance and contributing to a phase shift and thus an asymmetric spectrum [12] [17].

The effect is specifically evident for EER systems using a class-E as power amplifier configuration. As the switch is conducting, the output is pulled to ground and is therefore strict defined. However, when the switch is not conducting, the output is connected to the voltage supply. For a modulating PA, such as the case for EER, this voltage supply can drop below the level such that AM-PM conversion becomes evident.
In a class-D configuration, however, the output is hard switched to both ground and supply. This minimizes AM-PM as compared to a class-E configuration.

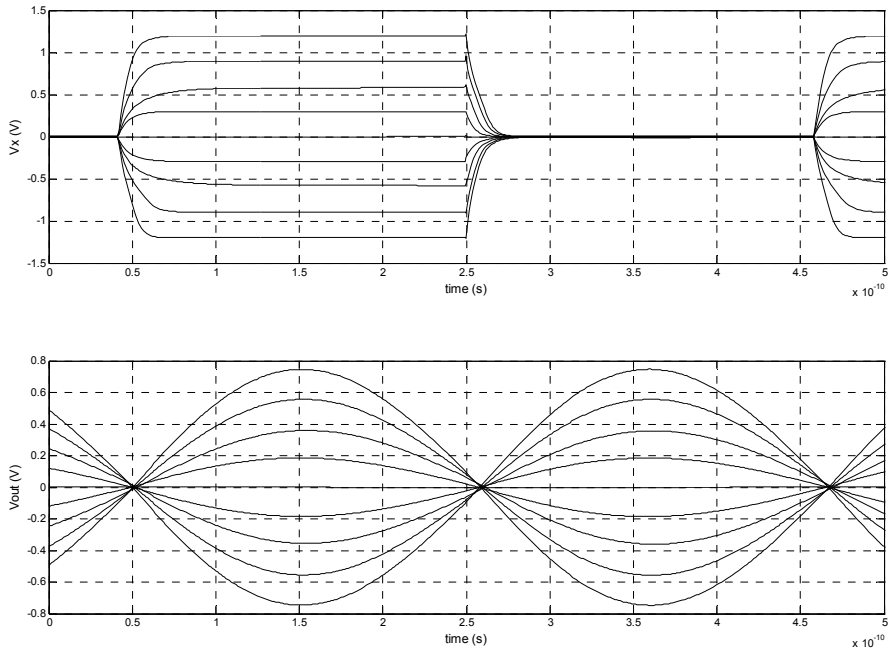

Figure 56 V_X and V_{out} for different I(t)

The topologies shown in §3.6 and §3.7 can be considered as class-D configuration, as the output is hard switched to either ground or supply. This means that this circuit is also less-sensitive for AM-PM conversion. Using the single end quadrature PA once more, Figure 56 shows simulated output for several RF periods for node V_X and V_{OUT} of a single end stage for different supply voltages. However, present in small amount, AM-PM conversion is present at the RF frequency. This can be seen by the fact that not all zero crossing at the output occur at the same time.

3.10. Driver

The quadrature PA consists of rather large devices, while any present driving signals are outputs of smaller minimum sized devices. To proper drive the quadrature PA, a dedicated buffer stage will be needed. Furthermore, the quadrature PA needs to be driven with a quadrature signal dependent polarity. Such a signal is assumed not readily available and thus needs to be generated. However, designing such a driver is not straight forward and gives rise to several issues. These will be discussed in §3.10.1 and based on these findings, a driver architecture and its specifications are given in §3.10.2.

3.10.1 Design issues of a quadrature PA driver

The quadrature PA from §3.6 and §3.7 is driven by a hard switching RF signal pulse signal which will be positive or negative depending on the sign of the quadrature signal I(t). When I(t) is positive the RF signal will be a pulse signal switching between zero (ground) and V_{DD}. If I(t) is negative signed, the RF signal will switch between V_{SS} and zero (ground). To construct such a signal, a possible driver topology such as Figure 57 could be used.

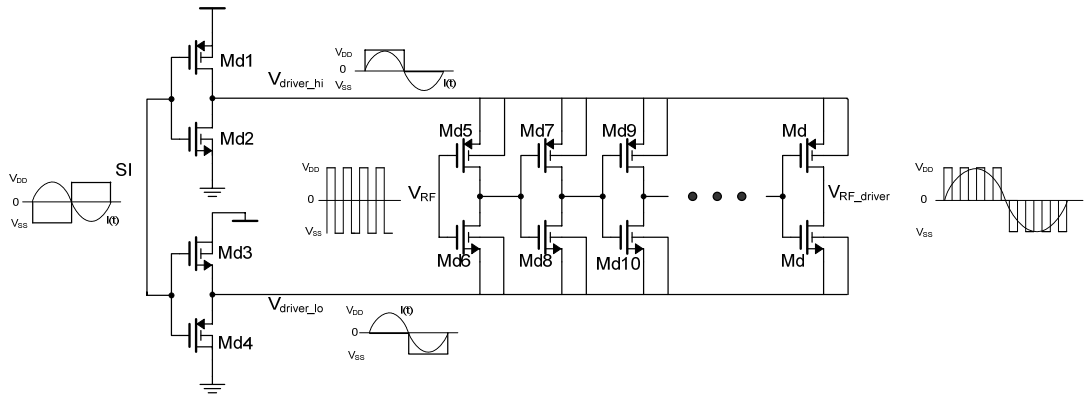

Figure 57 possible architecture for a single quadrature PA driver

The driver consists of a chain of inverter output stages and two set of switches. A quadrature signal parity bit SI(t), drives the two set of switches; one switches between V_{DD} and zero (ground) and the other between V_{SS} and zero (ground). The parity bit signal SI(t) is equal to V_{SS} when I(t) is signed positive and is equal to V_{DD} when I(t) is signed negative. An equivalent parity bit SQ(t) is assigned to the quadrature signal Q(t). The output of these set of switches function as the supply rails for the chain of inverters.

This chain is driven by a full swing RF signal V_{RF}, switching from the V_{DD} to V_{SS}. The output of the inverter chain V_{RF_driver} switches between the two output lines of the set of switches that are driven by SI(t). The result is that the output is thus the wanted RF hard switching signal as function of the quadrature signal I(t) and Q(t) sign.
It is assumed that a full swing RF signal and the quadrature parity bit signals SI(t) and SQ(t) are readily available.

However, driving such inverters with a full swing RF signal as $V_{RF,}$ the driver will inhabit a non-even output for positive and negative at the output. Suppose, I(t) is positive, thus SI is negative. In this case, the chain of inverters is switching between the V_{DD} and ground rails. If V_{RF} is high, i.e. V_{DD} then the NMOST of the first stage is conducting and the output is connected to the ground. However, if V_{RF} is low i.e. $V_{SS,}$ the PMOST is switched on, but with a relatively large overdrive voltage compared to the NMOST situation, pulling the output harder to V_{DD} rail than the NMOST can pull to ground. This will results in duty cycle larger than 50%. Now, if I(t) is negative, thus SI is positive, the same situation occurs, but opposite. The NMOST is turned on with a relatively higher overdrive voltage than the PMOST. Thus the NMOST pulls the output much harder to V_{SS} than the PMOST can pull to ground, resulting a duty cycle smaller than 50%.
The overall result is an uneven duty cycle that is opposite for positive and negative switching. This is illustrated in Figure 58, for 50% duty cycle V_{RF} input signal the positive output at V_{RF_driver} has an uneven duty cycle, which the high state duration is longer than the low state. For negative switching however, the low state duration is longer than the high state.

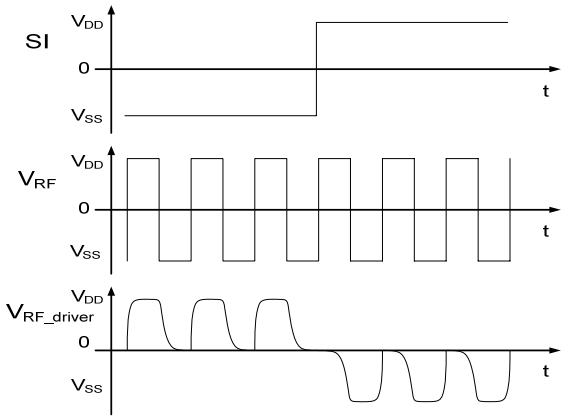

Figure 58 input and output signals for the driver architecture of Figure 57

The effects of this unbalanced driver output results in an uneven output for a single end quadrature PA, since its output is a direct function of the duty cycle. Conventionally, by changing the size of the transistors, the rise and fall times can be

set in such a way that a duty cycle of 50% can approximated. However, due to the opposite duality nature, if the duty cycle for positive switching approximates 50%, the negative side will not and vice versa. A simulated output of a driver as in Figure 57 is shown in the upper plot of Figure 59. The positive switching signal inhabits a duty cycle larger than 50%. Suppose this is corrected by decreasing the PMOST of the first stage. Shown in the lower plot of 58, the result is a duty cycle of 50%, but for the negative switching signal a larger PMOST will result in even lower duty cycle. These trade offs make it impossible to use an architecture as in Figure 57 if aimed for a 50% duty cycle, while using a full range switching signal as V_{RF} as driver input.

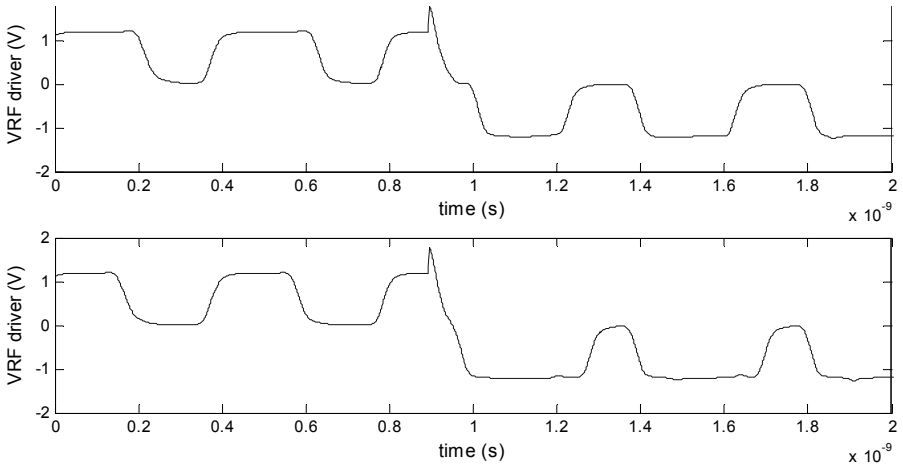

Figure 59 simulation result of output of driver as in Figure 57. Upper plot: uncorrected output. Lower plot: corrected for 50% duty cycle for positive switching

Another, but similar effect is the result of uneven rise and fall times. In a quadrature PA, both sides of the bridge are driven with the same signal, but with a 90° phase difference. If rise and fall times does not approximately equal the same duration, the signal “high” and “low” state does not correspond with this phase difference with respect to each other.

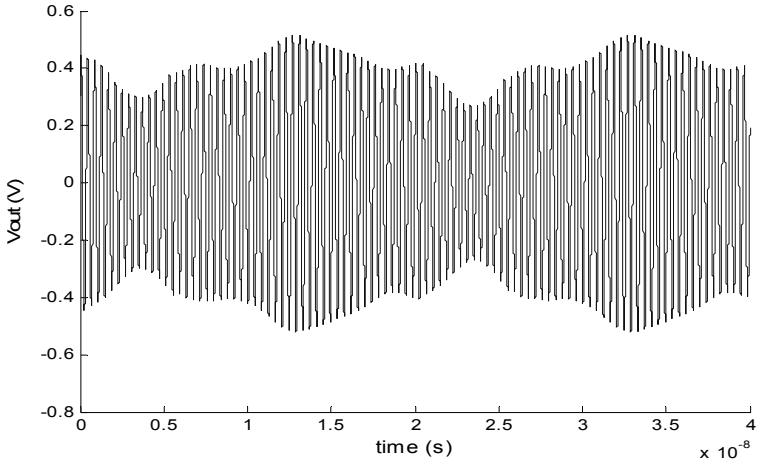

Figure 60 quadrature PA output for mismatch in driver signal for two message signal periods. The output envelope should be constant.

These two mismatch mechanism in the driver signal becomes evident in the quadrature PA output as shown in Figure 60. The output envelope should be constant, but it is not. This is because as each side is driven with an uneven driver signal, the output at each side of the bridge will be uneven as well. Subtracting these uneven signals which should be 90° out of phase will give different signal levels over time.

3.10.2 The quadrature PA driver

A way to overcome the aforementioned problems is to use a dedicated chain of inverters for only positive switching and one for only negative switching as illustrated in Figure 61. A switch passes either the positive or negative switching driver output to the quadrature PA, depending on the parity bit SI.

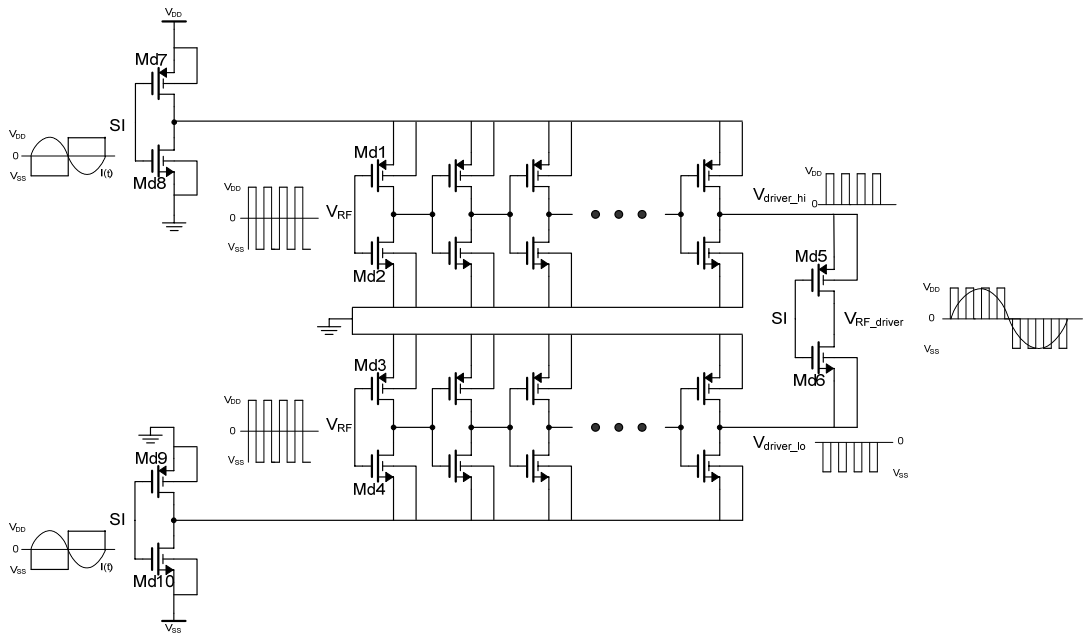

Figure 61 driver architecture for a quadrature PA

The advantage of using a topology as in Figure 61 is that the duty cycle and rise and fall times for either positive or negative switching can be set individually. Therefore the problem with duality between positive and negative switching is avoided. The downside however is increased chip area and power consumption. To limit the latter, switches consisting of inverter pair M_{d7} & M_{d8} and M_{d9} & M_{d10}, switches either chain of inverters off from the supply making them inactive. This will not affect its functionality, since only the output of either the positive or negative switching chain is desired.

The final inverter, consisting of transistor M_{d5} & M_{d6}, acts as a switch to pass either the positive or negative switching signal to the quadrature PA and consists of large thick gate oxide devices. Its width equals the same width as the devices of the quadrature PA.

Since the full swing RF signal V_{RF} and the parity bit signal switches between V_{DD} and V_{SS}, the gate source or gate drain voltages of the transistors that are driven by either V_{RF} or SI(t) can be twice the maximum allowed gate-source and gate-drain voltage. To solve this, thick gate oxide devices will be used for the transistors M_{d1} to M_{d10}. These allow a gate source or drain voltage of V_{Gtox}=2.5V
All the other devices in chain except the first stage are driven with a signal with a maximum voltage swing of 1.2V. Therefore, the gate source or gate drain voltages won't exceed the maximum allowable voltage and the faster minimal length devices of 90nm can be used in the RF signal path.

The first inverter stage in the chain is thus a larger, thick gate oxide device, while the others are 90nm devices. The second stage acts as coupling between the different devices.
The remaining stages of the chain of inverters acts as a consecutive increase of transistor width to proper drive the PA. This is because the available RF and other input signals are most likely outputs from signal processing circuits which use minimal size transistors, while the quadrature PA needs to deliver power and consists of much larger devices. Such a minimal size transistor is unable to drive a large size transistor directly and thus, this has to be done in certain steps of transistor size.
This implies that the transistor dimensions of the inverter chain, except for the first two stages, are determined by the transistor size of the input of the quadrature PA and the used step size and have therefore a fixed size. This leaves only the first two stages left to dimension. This is achieved by means of tuning transient output to approximate 50% duty cycle for both positive and negative switching and keeping the rise times approximately equal to the fall times.
The resulting driver output compared to the full swing input signal V_{RF} is shown in Figure 62 for different stepsizes. It can be seen that that up to a stepsize of N=9, the output gives a pulse signal with approximate equal duty cycle and rise and fall times for both positive and negative switching. However, for a stepsize of N=10 or larger, the driver fails to generate an output at all. Note that, since an even and uneven numbers of inverter stages are used, the shown output signal also shows inverted version of the output signal.

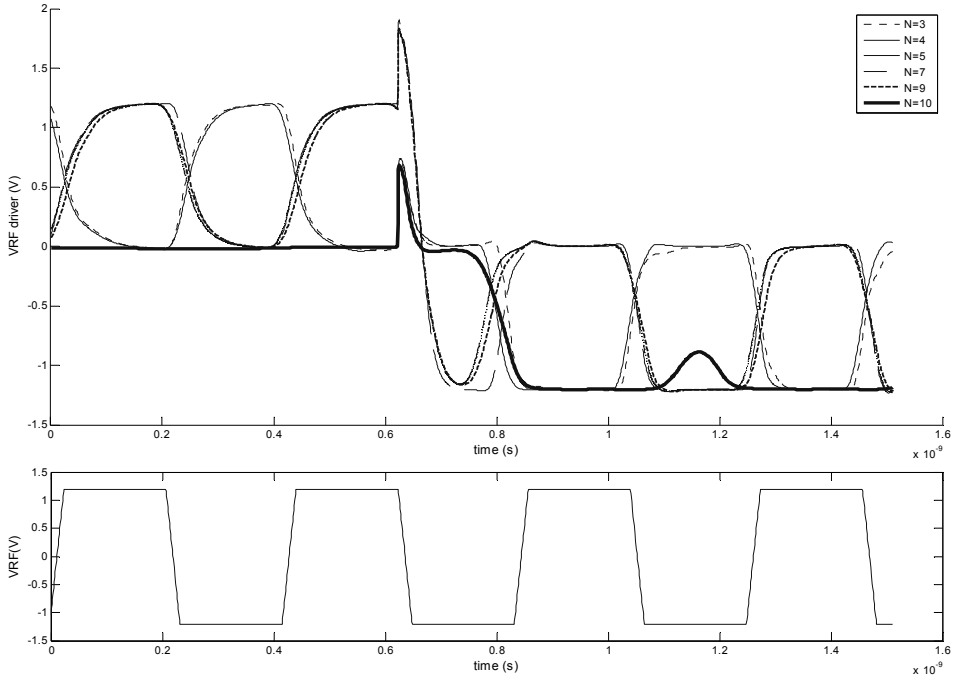

Figure 62 driver output for step size N=3, 4, 5, 7, 9, 10 for both positive and negative switching

Since each stage will introduce its own losses as conduction and switching losses, limiting the number of stages is required to maintain high power efficiency. However, choosing a too low step size the driver won't be able to drive its stages. There is thus an optimum between power efficiency and functionality. For several step sizes the power efficiency/consumption is shown in Figure 63 and Table 6.
The power consumption is calculated as the power dissipation of each transistor for a large number of periods averaged over time. Both positive and negative switching of equal duration are taken into account.
As a comparison the power consumption for both with and without the voltage supply switches M_{d7}, M_{d8}, M_{d9} and M_{d10} is presented. Though only one chain is active, these switches are relatively large, since they have to be able to conduct currents from the supply to all inverter stage, dissipating a relatively large amount of power by ohmic and parasitic capacitive losses. The result is diminishing of only about a third of the power consumption using these supply switches.
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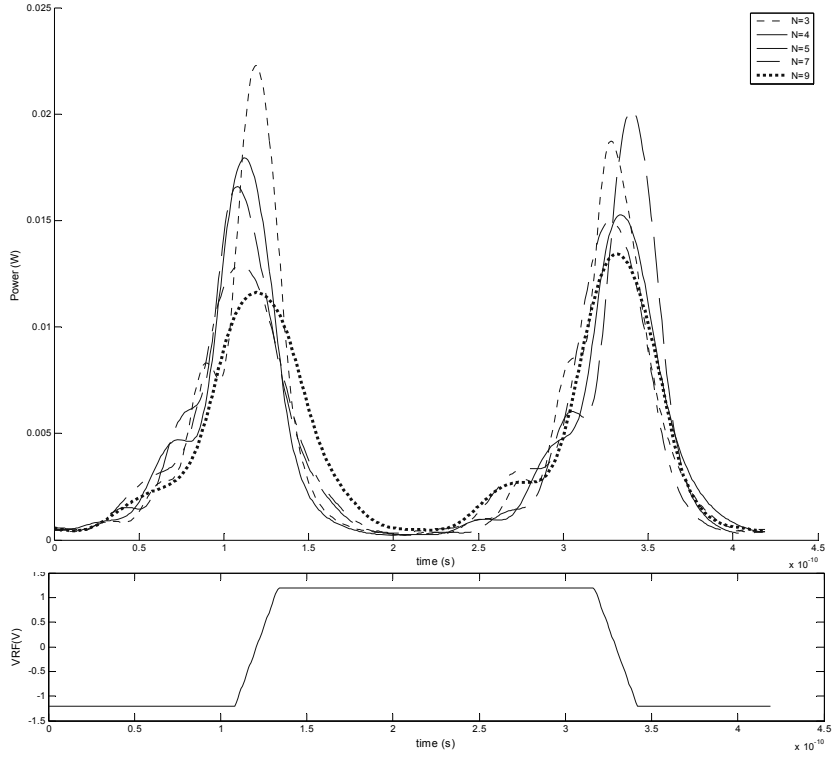

Figure 63 power consumption of the driver for one RF cycle for step size N=3, 4 , 5, 7, 9

step size N	number of inverter stages	power without supply switches M_{d7}, M_{d8}, M_{d9}, M_{d10}	power with supply switches M_{d7}, M_{d8}, M_{d9}, M_{d10}
3	8	7.56 mW	4.86 mW
4	7	7.07 mW	4.64 mW
5	6	6.73 mW	4.39 mW
6	6	6.65 mW	4.36 mW
7	5	6.63 mW	4.37 mW
8	5	6.63 mW	4.36 mW
9	5	6.62 mW	4.33 mW
10	5	-	-

Table 6 power consumption of the driver for different stepsize. The number of stages includes the number of inverter stages of the total chain of inverter including the first two stages.

As expected it shows, that a higher step size corresponds with lower power consumption. However, from transient results it also becomes clear that a too high a step size results in a non proper drive of the quadrature PA, i.e. the driver is unable to generate a pulse shaped waveform. Thus, for minimal power consumption by the driver, while maintaining the ability to proper drive the quadrature PA a step size of N=9 is chosen, which corresponds to 5 stages.

To drive the quadrature PA properly, four of these drivers are needed. In a quadrature PA, both sides of the bridge needs its own driver set, driving with 90° phase difference, while each single end quadrature PA on either side of the bridge needs two drivers running an inverted driving signal with respect to each other. This means that the total power consumption of all the drivers will be four times as noted in Table 6.

4. Simulations

4.1. Introduction

The quadrature power amplifier is designed for wireless applications, though no specific application requirements are needed, the aim is the use for IEEE 802.11 standards such as WLAN. This protocol requires an RF carrier frequency of F_{RF}=2.4GHZ

All simulations are performed using the CADENCE SPECTRE simulation software. Unless otherwise noted, the simulations are run at "errpreset" set at conservative and all other options at default. The results are imported and plotted in Matlab for viewing purposes.

The following paragraphs deal with the used models and technology (§4.2), the component dimensions (§4.3) and the used testbench for the simulations (§4.4). The simulations results are shown at the end (§4.5) and are sorted per testbench.

4.2. Technology and models

The quadrature power amplifier is designed for a 90nm CMOS process and a voltage supply of V_{DD}=1.2V and V_{SS}=-1.2V. Simulations are performed using the UMC90nm library. Table 7 shows the used models of this library. Table 8 shows the general components used from standard CADENCE libraries.

model name	type	min. chann. length	notes
12Nmost LLVT	NMOST	90nm	Low leakage low threshold voltage device
12Pmost LLVT	PMOST	90nm	Low leakage low threshold voltage device
25Pmost	NMOST	240nm	2.5V operating voltage
25Pmost	PMOST	240nm	2.5V operating voltage
Mimcaps_20f_mm	capacitor	-	Metal insulator metal structure

Table 7 used models of the UMC90nm library

modelpart	library	notes
source	analoglib	
inductor	analoglib	inductor resistance = 0Ω
capacitor	analoglib	
resistance	analoglib	
switch	analoglib	switch resistance = 1mΩ
comparator	functional	gain = 1000
opamp	functional	gain = 1000

Table 8 used models of the analoglib and functional libraries

4.2.1 Signal set

The following signals are assumed to be readily available, Table 9.

signal name	value	rise and fall times	phase
V_{DD}	1.2V	-	-
V_{SS}	-1.2V	-	-
I(t)	Quadrature signal		0°
Q(t)	Quadrature signal		90°
VRFI	even pulse signal between 1.2V and -1.2V	t_{rise} = 160fs t_{fall} = 160fs	0°
$\overline{VRFI}$	even pulse signal between 1.2V and -1.2V	t_{rise} = 160fs t_{fall} = 160fs	180°
VRFQ	even pulse signal between 1.2V and -1.2V	t_{rise} = 160fs t_{fall} = 160fs	90°
$\overline{VRFQ}$	even pulse signal between 1.2V and -1.2V	t_{rise} = 160fs t_{fall} = 160fs	270°
SI	1.2V when I(t) < 0V -1.2V when I(t) > 0V	t_{rise} = 8.5ps t_{fall} = 8.5ps	-
SQ	1.2V when Q(t) < 0V -1.2V when Q(t) > 0V	t_{rise} = 8.5ps t_{fall} = 8.5ps	-

Table 9 readily available signal set

For simulation purposes the four hard switching RF will have to be generated. This is done using a setup as shown in Figure 64.

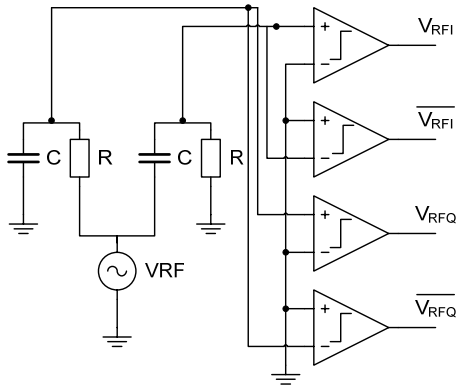

Figure 64 generation of the driver RF input signals

A sinusoidal voltage source at RF frequency driving an RC-CR filter, results in two harmonic signals which differ 90° in phase. The RC-CR filter is tuned to the proper frequency of f_{RF}=2.4GHz by:

$$f_{RF} = \frac{1}{2\pi}\frac{1}{\sqrt{RC}} \tag{20}$$

With R=1KΩ and C=66fF.
A set of ideal comparators, with a gain of A=1000 and the threshold level set at ground, transforms the sinusoidal signals to hard switching, even pulse signals. For each of the two sinusoidal signal a pulse signal is generated with the same phase or an inverted phase. The result is the wanted four driver input RF signals.

The parity bit signals SI and SQ are generated using the same ideal comparators as shown in Figure 65. The input signals are the quadrature signals I(t) and Q(t) respectively. Note that the input is connected to the negative input of the comparator as the parity bit signals are negatively signed with respect to the quadrature signals sign.

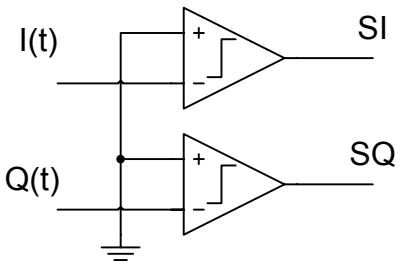

Figure 65 generation of the parity bit signals SI and SQ

4.3. Device and component dimensions

4.3.1 Introduction

For the following simulations, transistor dimensions and component values for the quadrature PA without bulk switches are shown in §4.3.2 and for the quadrature PA with bulk switches are shown in §4.3.3.
Both setups use the same driver, which is configured as §4.3.4. The driver will be executed in fourfold to properly drive the quadrature PA.

4.3.2 Quadrature PA without bulkswitches

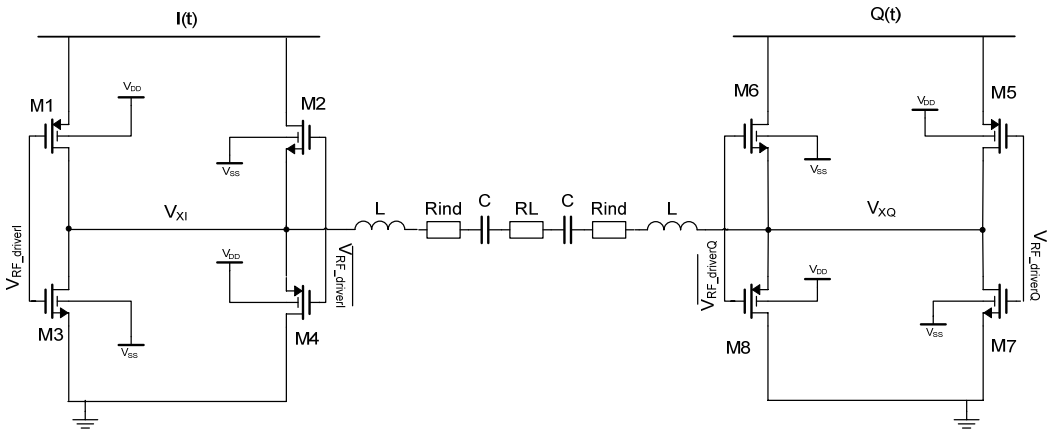

Figure 66 simulation setup of quadrature PA without bulkswitches

device number	model	length	width
M1, M5	12Pmost LLVT	90nm	150µm
M2, M6	12Nmost LLVT	90nm	100µm
M3, M7	12Nmost LLVT	90nm	100µm
M4, M8	12Pmost LLVT	90nm	150µm

Table 10 device parameters for quadrature PA without bulkswitches

component	model	value
L	inductor	33nH
R_{ind}	resistor	200mΩ
C	Mimcaps_20f_mm	133fF
R_L	resistor	50 Ω

Table 11 component values of load network for quadrature PA without bulkswitches

4.3.3 Quadrature PA with bulkswitches

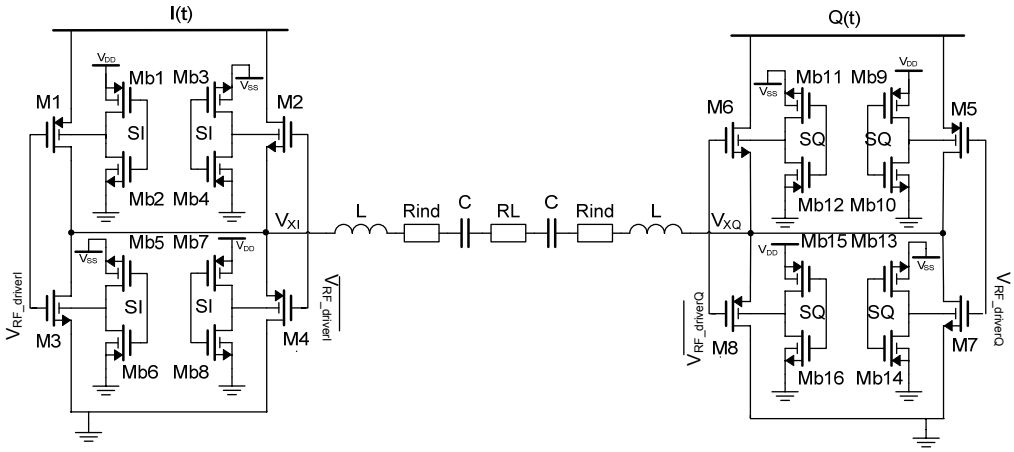

Figure 67 simulation setup of quadrature PA with bulkswitches

device number	model	length	width
M1, M5	12Pmost LLVT	90nm	150µm
M2, M6	12Nmost LLVT	90nm	100µm
M3, M7	12Nmost LLVT	90nm	100µm
M4, M8	12Pmost LLVT	90nm	150µm
Mb1, Mb4,Mb6, Mb7	25Pmost	240nm	360nm
Mb2, Mb3,Mb5, Mb8	25Nmost	240nm	360nm
Mb9, Mb12,Mb14, Mb15	25Pmost	240nm	360nm
M10, Mb11,Mb13, Mb16	25Nmost	240nm	360nm

Table 12 device parameters for quadrature PA with bulkswitches

component	model	Value
L	inductor	33nH
R_{ind}	resistor	200mΩ
C	Mimcaps_20f_mm	133fF
R_L	resistor	50 Ω

Table 13 component values of load network for quadrature PA without bulkswitches

4.3.4 Driver

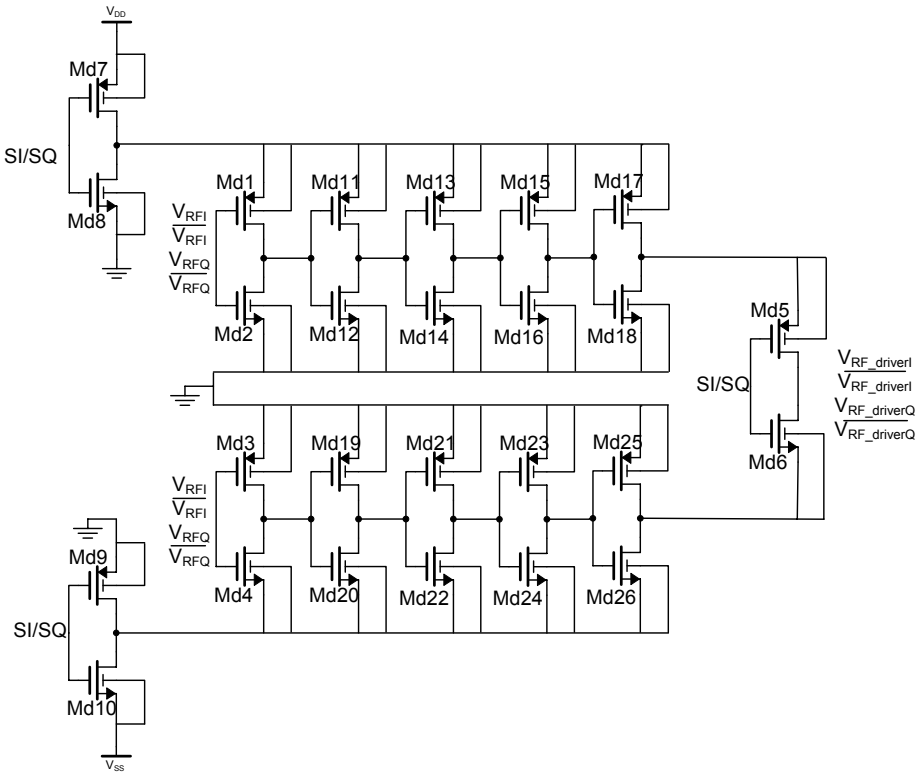

Figure 68 simulation setup of the driver

device number	position	model	length	width
M_{d1}	stage 1	25Pmost	240nm	360nm
M_{d3}	stage 1	25Pmost	240nm	1.9µm
M_{d2}, M_{d4}	stage 1	25Nmost	240nm	360nm
M_{d5}	output switch	25Pmost	240nm	150µm
M_{d6}	output switch	25Nmost	240nm	100µm
M_{d7}, M_{d9}	supply switch	25Pmost	240nm	500µm
M_{d8}, M_{d10}	supply switch	25Nmost	240nm	400µm
M_{d11}, M_{d19}	stage 2	12Pmost LLVT	90nm	600nm
M_{d13}, M_{d21}	stage 3	12Pmost LLVT	90nm	2.1µm
M_{d15}, M_{d23}	stage 4	12Pmost LLVT	90nm	17µm
M_{d17}, M_{d25}	stage 5	12Pmost LLVT	90nm	150µm
M_{d12}, M_{d20}	stage 2	12Nmost LLVT	90nm	360nm
M_{d14}, M_{d22}	stage 3	12Nmost LLVT	90nm	1.2µm
M_{d16}, M_{d24}	stage 4	12Nmost LLVT	90nm	11nm
M_{d18}, M_{d26}	stage 5	12Nmost LLVT	90nm	100µm

Table 14 device parameters for driver

4.4. Testbench

4.4.1 Introduction

For both the quadrature with and without the bulk switches the following simulations will be performed to test functionality and performance.

4.4.2 Transient

A transient simulation will be performed to check the quadrature PA's functionality. The quadrature signals I(t) and Q(t) will be set as sinusoid as shown in Figure 69. The envelope at the quadrature PA output should be constant. A not constant envelope can be attributed to mismatch in the driver and/ or in the PA.

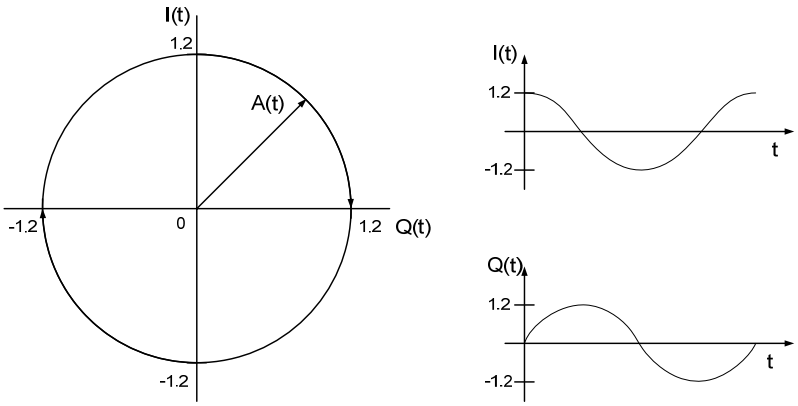

Figure 69 IQ-constellation for transient simulation

To exclude the effect of the driver, a similar simulation will be performed using fast switching, low loss switch models as ideal driver as found in Table 8.

4.4.3 Quasi-periodic steady state analysis

Using the same IQ constellation signal set as Figure 69 for the transient analysis, the power spectrum of the output of the quadrature PA will be simulated using a quasi-periodic steady state analysis. As shown, the output will be shifted up in frequency and the carrier will be suppressed. Of interest is the strength of this carrier suppression is and the 3rd intermodulation product of the signal output and the carrier.

For simulation convergence reasons the supply rails of the driver bypasses the supply switches and are directly connected to either V_{DD} or V_{SS}.

4.4.4 16-QAM analysis

A second transient simulation will be performed in a 16-QAM manner. Two periodic discrete level signals with the same frequency make up an IQ constellation as shown in Figure 70. For each period, the output should follow the amplitude of each constellation point as numbered, starting with 0000 and ending with 1111. Each level has a duration of 10ns, the total period is thus T=160ns. Switching times of I(t) and Q(t) are assumed infinite fast.

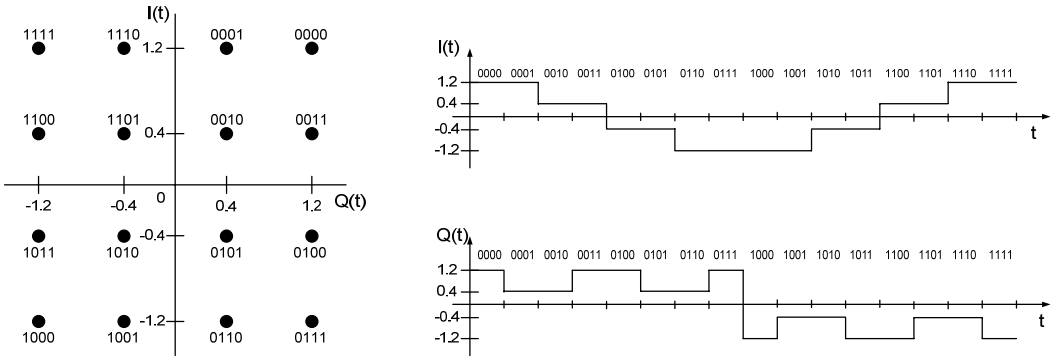

Figure 70 IQ-constellation for 16-QAM like transient simulation

Since no IQ-mismatch will be simulated, any deviation in symmetry will be contributed by the quadrature PA and driver capability of handling negative voltages with respect to positive voltages. The output envelope will have to consist of three levels. A spreading, the relative difference between the highest and lowest amplitude is a measure on how symmetrical the quadrature PA is.
To exclude the effect of the driver, a similar simulation will be performed using fast switching, low loss switch models as driver. The difference in output is a measure on how well the driver acts compared to an ideal driver.

4.4.5 Output bandwidth

Using a quasi-periodic AC analysis simulation, the output bandwidth is simulated. The input quadrature signals I(t) and Q(t) are sinusoidal with an amplitude of 1.2V. As the output will a shifted translation with respect to the carrier frequency, a transfer function can be constructed. The output should take the form of Figure 22. Of interest is the maximum amplitude and the -3dB bandwidth frequency. This

should be around the RF-frequency divided by the Q factor of the LCR load filter i.e. $1/Q * f_{RF} = 240MHz$.
For simulation convergence reasons the supply rails of the driver bypasses the supply switches and are directly connected to either V_{DD} or V_{SS}.

4.4.6 Power added efficiency

The power added efficiency (PAE) is found as:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{21}$$

With P_{out} the power at the output of the PA, P_{in} the power delivered by the driver and P_{dc} the power delivered by voltage sources V_{DD}, $V_{SS,}$ I(t) and Q(t).
The quadrature signals I(t) and Q(t) are set at an alternating amplitude of maximum 1.2V or minimum 1.2V, the quadrature PA is delivering power at maximum input. The resulting IQ constellation is shown in Figure 71 and the quadrature PA output will follow the amplitude of A_1 to A_4 in a switching manner at 10MHz and 50MHz.

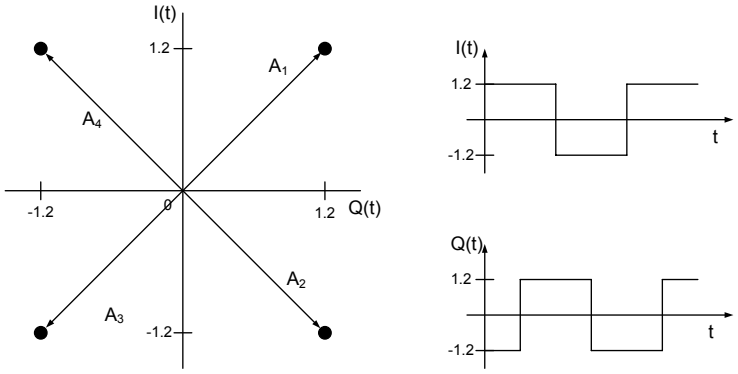

Figure 71 IQ-constellation for PAE simulation

4.5. Simulation Results

The following paragraph is divided in five parts. Each part of §4.5.1 - §4.5.5 summarizes the simulation results of respectively the quadrature PA without and with bulkswitches for each of the simulation as given in §4.4.

4.5.1 Transient simulation results

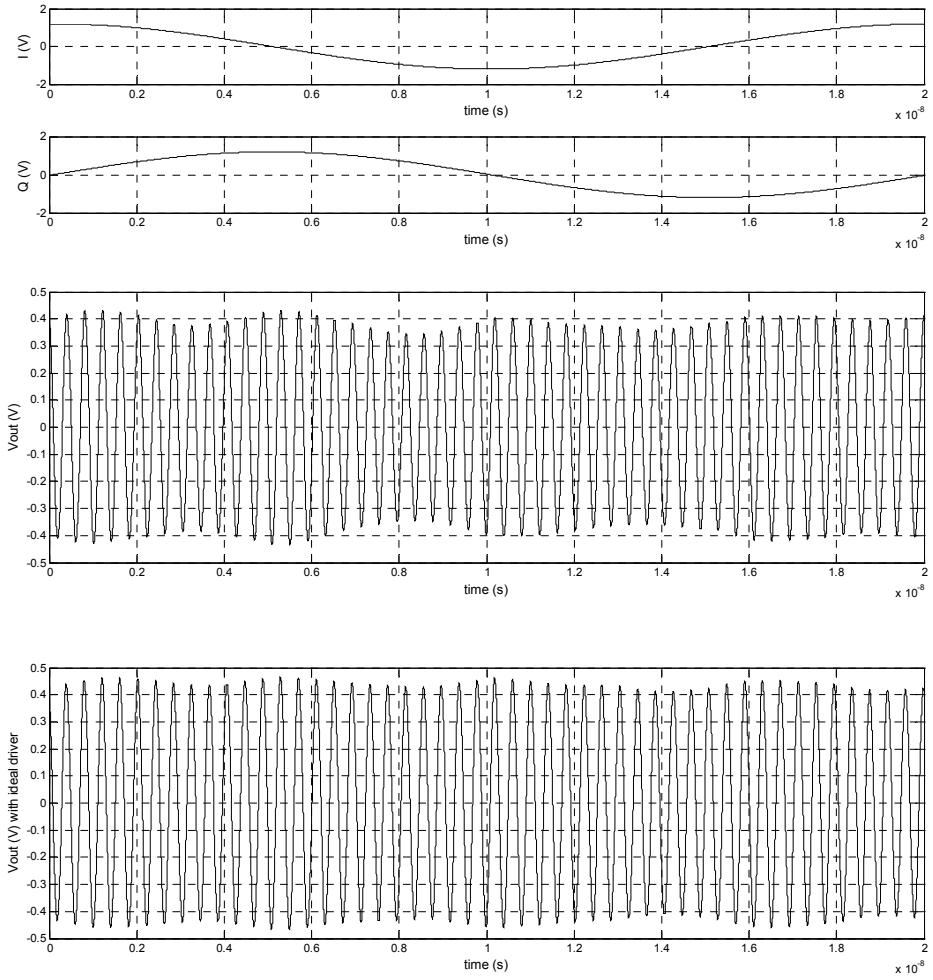

Figure 72 simulations results for the quadrature without bulkswitches, Vout (middel) and Vout with ideal drivers (lower) with I(t) and Q(t) sinusoid at 50MHz

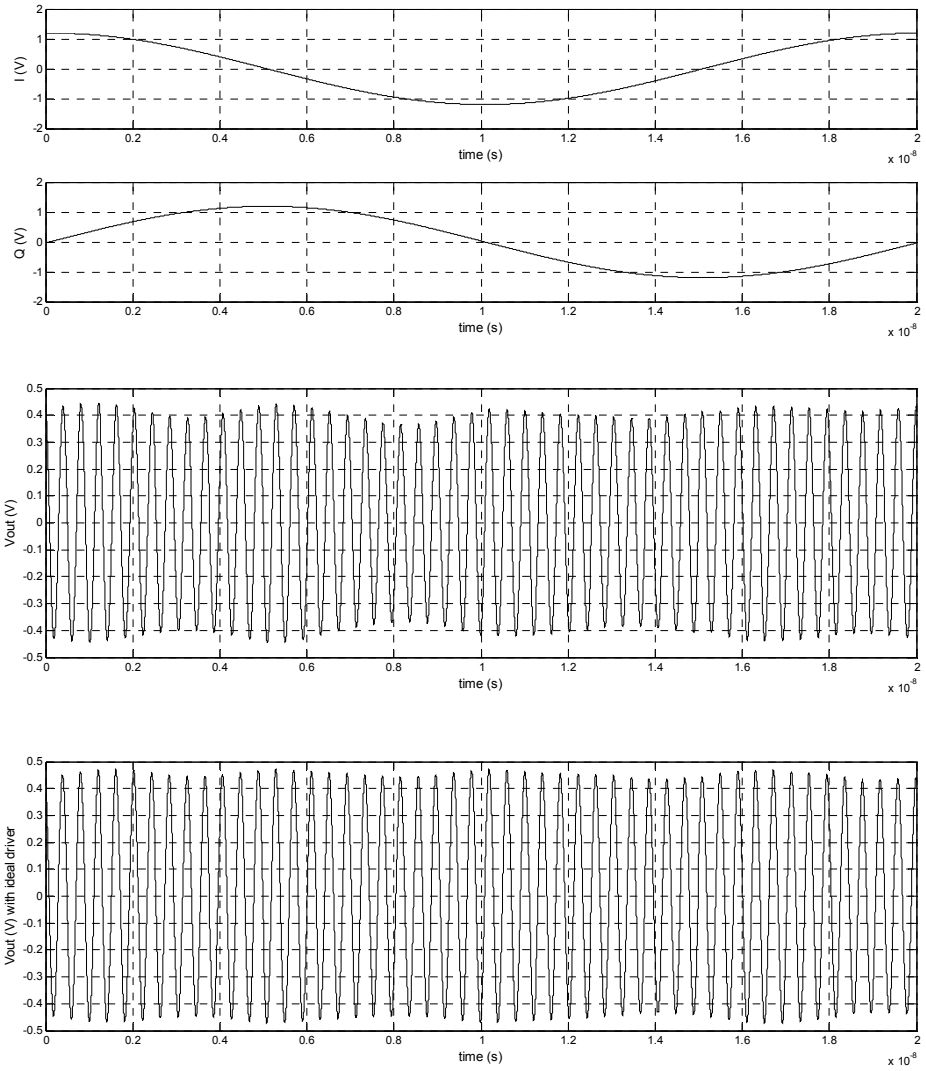

Figure 73 simulations results for the quadrature with bulkswitches, Vout (middel) and Vout with ideal drivers (lower) with I(t) and Q(t) sinusoid at 50MHz

Shown in Figure 72 and Figure 73 are the transient results of respectively the quadrature PA without and with bulkswitches. As a comparison the output using an ideal driver is shown as well. Both quadrature PA designs show almost identical output, with the output of the quadrature PA with bulkswitches having a slightly larger peak to peak output voltage.

At a glance, the output is indeed the expected RF carrier with constant amplitude, but the envelope shows a periodic “ripple” as it is not flat. This can be seen at the output using either the driver or the ideal driver. Though a not constant envelope

indicates an incorrectly functioning system, this ripple is caused by computational resolution errors by the post processor of the simulator. As the frequency of the output is shifted up in frequency, the sampling frequency of the simulator is not. The result is that the output is not reconstructed correctly.

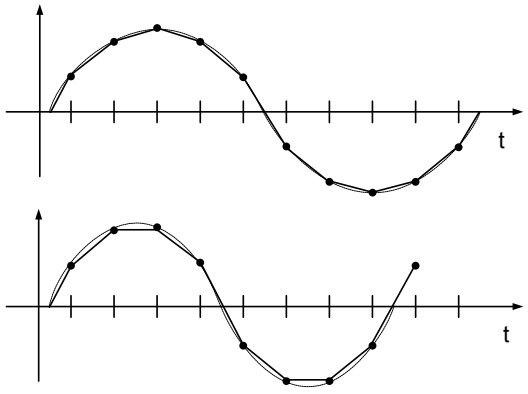

Figure 74 reconstruction error by the post simulator. Upper plot shows the ideal (dotted) and correct sampled (direct) signal. Below, for the same signal with a higher frequency, the correct signal (dotted) and the reconstructed signal (direct). Sample moments are denoted by the dots.

Suppose the period of the sampled signal in the upper plot of Figure 74. As this signal goes up in frequency, while the sample frequency is not, the signal should be reconstructed as the dotted line of the lower plot. Instead, the simulator reconstructs the signal as the direct line. The result is that the peak value can be higher or lower than the actual signal. Though the difference is minimal, it is noticeable at the outputs envelope as it shows moments of increased and decreased amplitude, resulting in the periodic ripple.

Though the results of the quadrature with and without the driver are almost identical, if looked closely, the amplitude of the output using the driver is not periodic. For both the quadrature PA with and without bulkswitches the envelope show a dip at t=8ns. This indicates that the driver for this operating region of I(t) and Q(t) is not operating symmetrically with respect to the other operating regions. Paragraph § 4.5.3 will go into this with more detail.

4.5.2 Quasi-periodic steady state simulation results

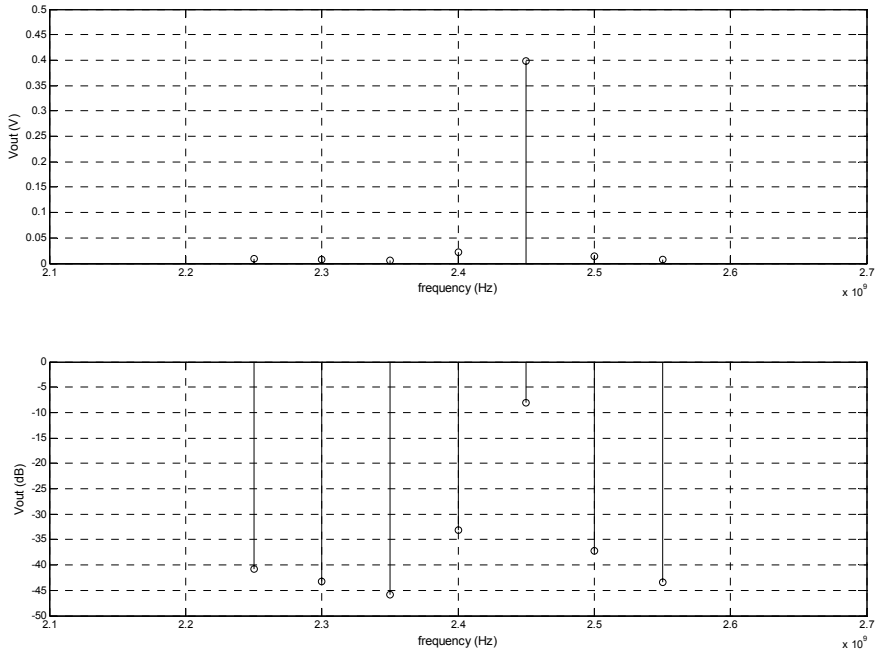

Figure 75 QPSS spectrum simulations results for the quadrature PA without bulkswitches, Vout in Volts (upper) and decibel (lower) with I(t) and Q(t) sinusoid at 50MHz

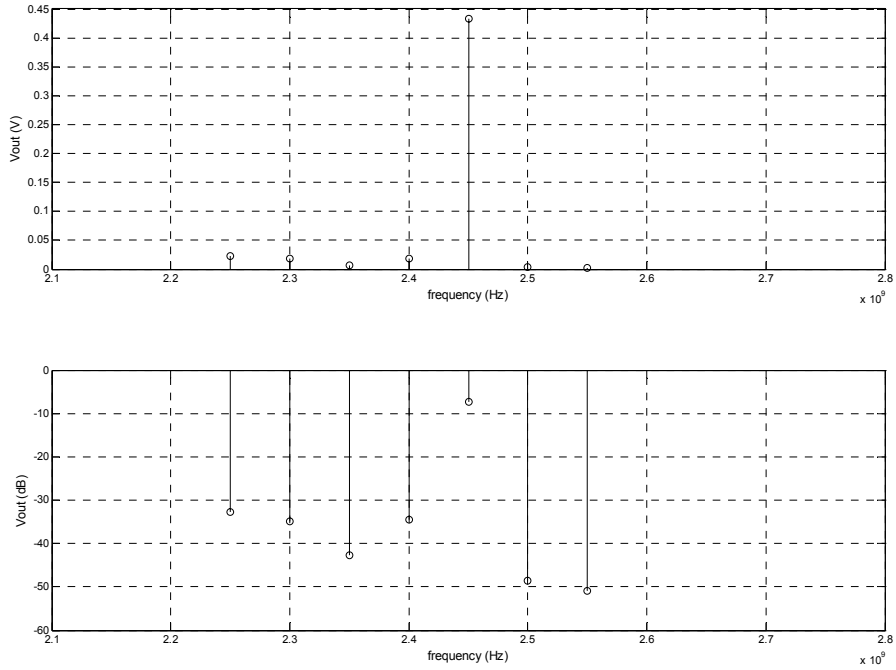

Figure 76 QPSS spectrum simulations results for the quadrature PA with bulkswitches, Vout in Volts (upper) and decibel (lower) with I(t) and Q(t) sinusoid at 50MHz

		quadrature PA without bulkswitches		quadrature PA with bulkswitches	
expression	**frequency (Hz)**	**magnitude (V)**	**magnitude (dB)**	**magnitude (V)**	**magnitude (dB)**
f_{signal}	2.45G	397.68m	-8.01	432.59m	-7.28
$f_{carrier}$	2.40G	22.142m	-33.19	18.77m	-34.53
$2f_{carrier}-f_{signal}$	2.35G	5.10m	-45.85	7.29m	-42.74
$2f_{signal}-f_{carrier}$	2.50G	13.77m	-37.22	3.76m	-48.49

Table 15 QPSS spectrum simulation output magnitude

Both the quadrature PA with and without the bulkswitches show the same single sideband suppressed carrier characteristic as expected. As the quadrature PA with bulkswitches has a higher peak voltage output, the suppression of the 3rd order intermodulation frequency of the signal with the carrier is also higher.

4.5.3 16-QAM simulation results

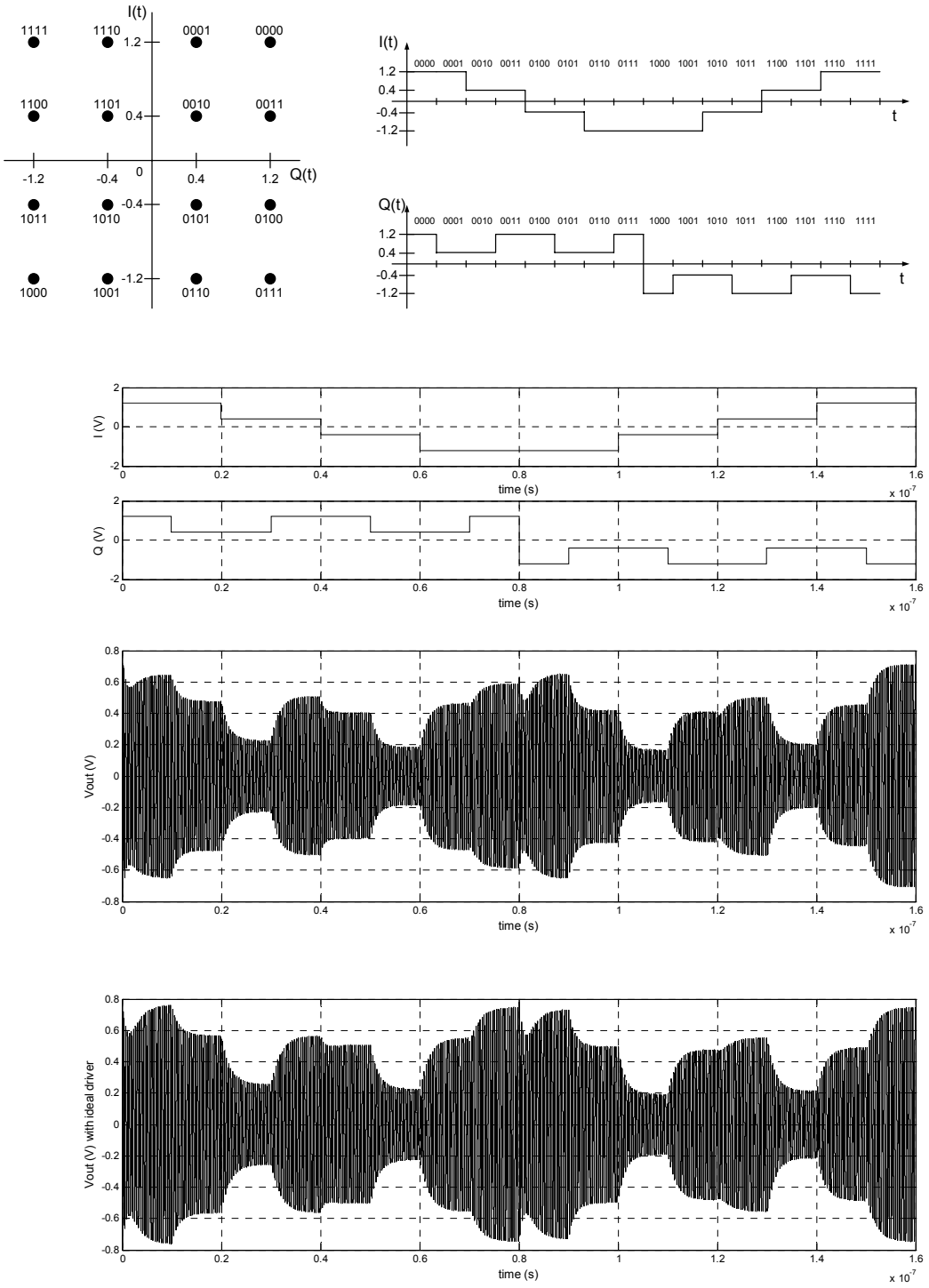

Figure 77 simulations results for the quadrature PA without bulkswitches Vout (middle) and Vout with ideal drivers (lower) with I(t) and Q(t) at16QAM operation

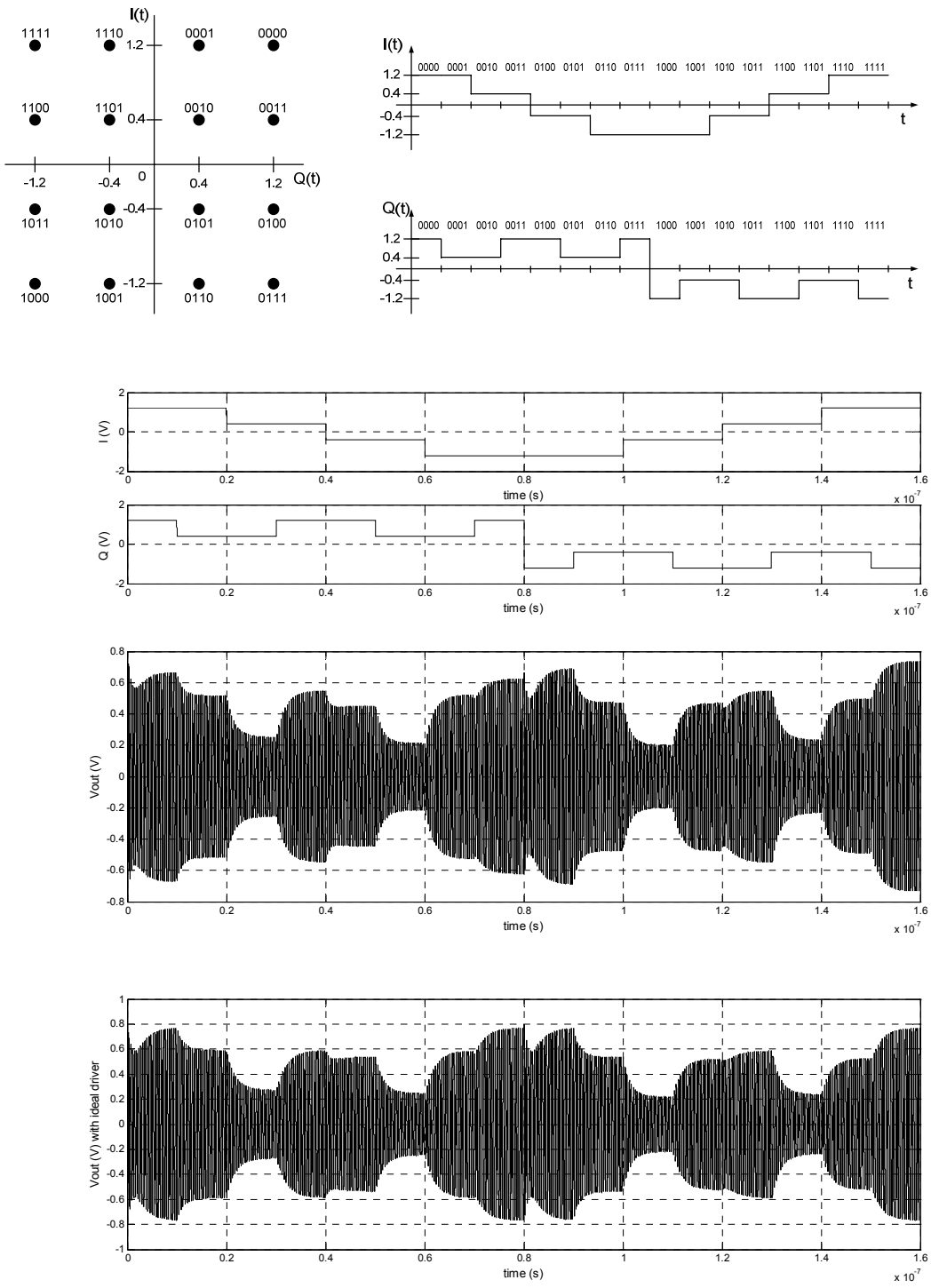

Figure 78 simulations results for the quadrature PA with bulkswitches, Vout (middle) and Vout with ideal driver (lower) with I(t) and Q(t) at 16QAM operation

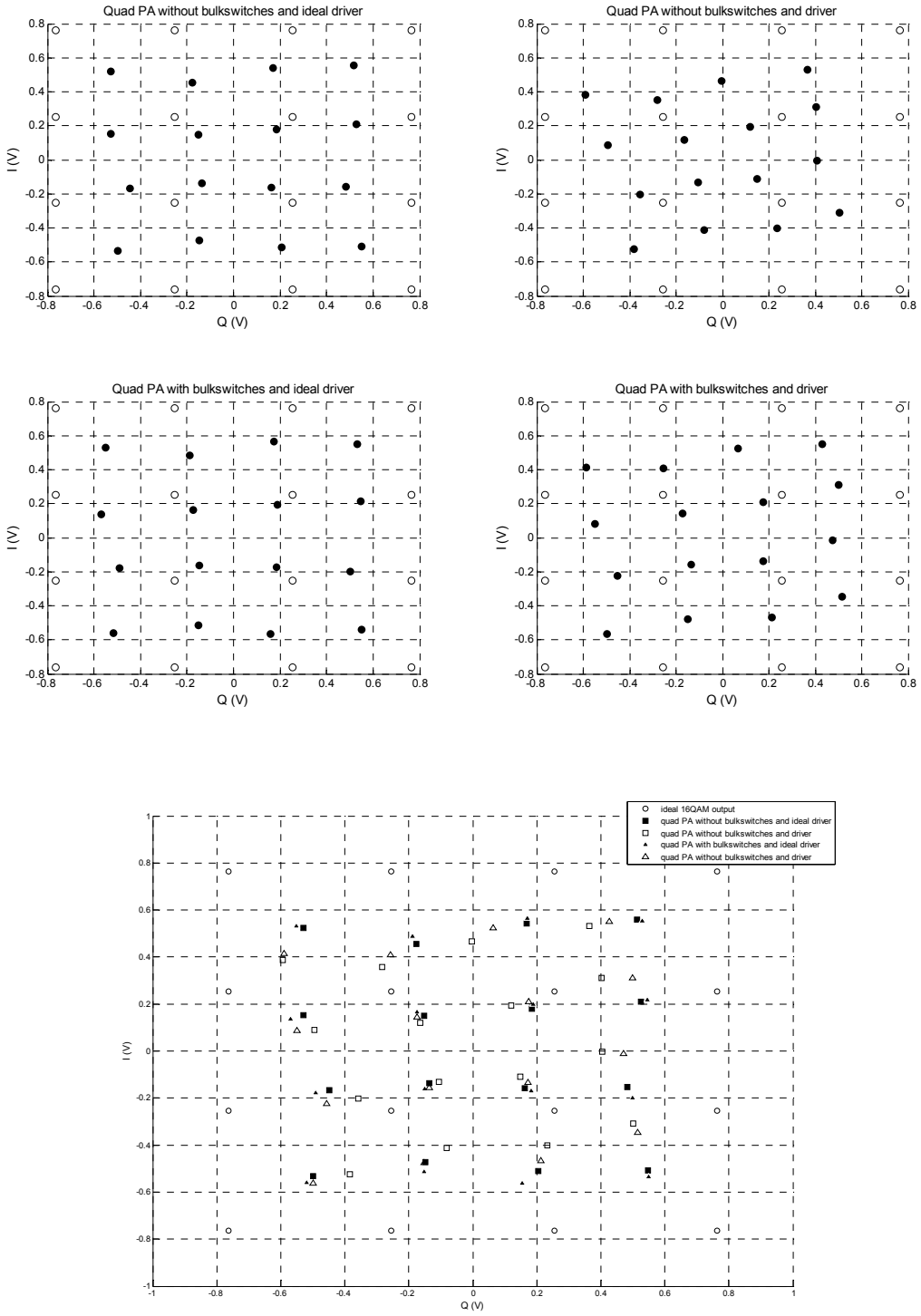

Figure 79 IQ-constellations of 16QAM simulation results, the open circle denotes the ideal 16QAM output

Shown in Figure 77 and Figure 78 are the transient simulation results for the 16QAM simulation for respectively the quadrature PA without and with bulkswitches. Also shown is the output using an ideal driver. The results are for both quadrature PA designs almost identical. The same deviation of elements can be found in both designs output, for example element 0100 and 1011. The difference lies in the fact that the output for the quadrature PA with bulkswitches has a larger magnitude.

Shown in Figure 79 are the reconstructed IQ-constellation plots of the output. For every plot, the ideal output is denoted by an open circle. It shows that the output is a scaled down version of the ideal output. This is because, as the proper size of the transistors a trade-off between voltage signal waveform and power efficiency is made. As a result the devices of the quadrature PA exhibit considerable ohmic losses that corrupts the hard switching pulse RF signal, as shown in §3.8.4. Though the efficiency is maximized, the voltage signal waveform is thus deformed as shown in Figure 54. As stated in §3.4, the output amplitude is dependent of the voltage signal waveforms and drops as the shape is not a strict pulse signal. The result is thus an attenuated output voltage.

Suppose element 0000. The ideal magnitude of this element is $A_{0000}=\sqrt{(I^2(t)+Q^2(t))}=\sqrt{(1.2^2+1.2^2)}=1.07V$. Using the simulation results for this same element, the voltage attenuation at the output can be found, assuming that the simulated phase output is correct. Listed in Table 16 as the scaling factor, this factor is used as an approximation to compensate for the attenuation. The result is a 16QAM output IQ-constellation, which makes a comparison with the ideal output easier.

	quadrature PA without bulkswitches		**quadrature PA with bulkswitches**	
	ideal driver	**driver**	**ideal driver**	**driver**
ideal magnitude	1.07 V	1.07 V	1.07 V	1.07 V
simulated magnitude	751.02 mV	645.18 mV	767.12 mV	664.28 mV
scaling factor	1.42	1.66	1.39	1.61

Table 16 amplitude scaling factor for 16QAM simulation

These compensated output IQ-constellation plots can be found in Figure 80. Using an ideal driver, the quadrature PA with bulkswitches performs slightly better than the quadrature PA without bulkswitches as the output of the former has eight elements which overlap the ideal output, while the latter has seven overlapping elements. Also, the quadrature PA with the bulkswitches has slightly smaller errors between the simulated and ideal output.

The output plots of the quadrature PAs using the driver show a phase change, in such a way that the total constellation is shifted with positive phase with respect to

the positive x-axis. The driver introduces thus a positive phase shift, which is about 15°. This phase shift is introduced as the driver output has finite rise and fall times. Any parasitic capacitances of the quadrature PA will be charged and uncharged for a length of time, resulting in the phase shift. An ideal driver, with its hard, infinite fast switching behavior will also charge and uncharge these parasitic capacitances infinite fast, that there is a minimal phase shift.

The final plot of Figure 79 and Figure 80 show all the output in one plot. As the output of the quadrature Pas using an ideal driver fairly coincides with each other, the output of the designed driver is not, because of the introduced phase shift.

The non-accurate mapping of the output can be contributed to the fact that the on-resistance of the devices varies with the input. As shown in §3.7, the on-resistance is a non-linear function of the input. The result is that the output varies in magnitude and phase as function of the input. The first is logical. The phase variations can be contributed, besides the AM-PM distortion as mentioned in §3.9, to the fact that the on-resistance and parasitic capacitances introduces phase shifts. Using bulkswitches the variation of the on-resistance is reduced and simulation results of the quadrature PA with bulkswitches show indeed an improvement in results. However, for practical application this will highly likely not be sufficient. As a more complex modulation scheme is used, such as 128QAM or 256QAM for multiple channel applications, the error shown in Figure 79 and Figure 80 will have to be reduced.

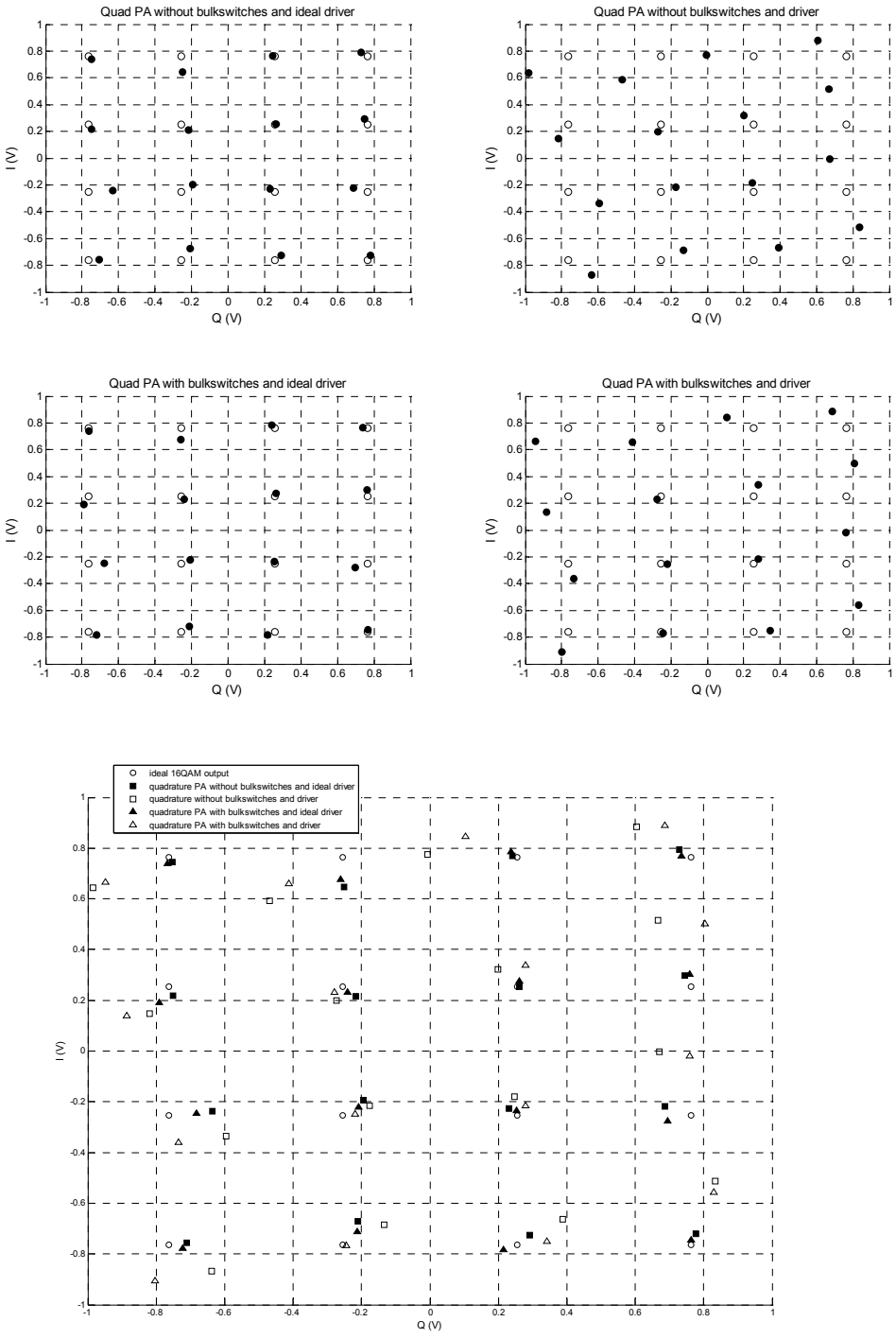

Figure 80 output magnitude compensated IQ-constellations of 16QAM simulation results, the open circle denotes the ideal 16QAM output

4.5.4 Quasi-periodic AC simulation results

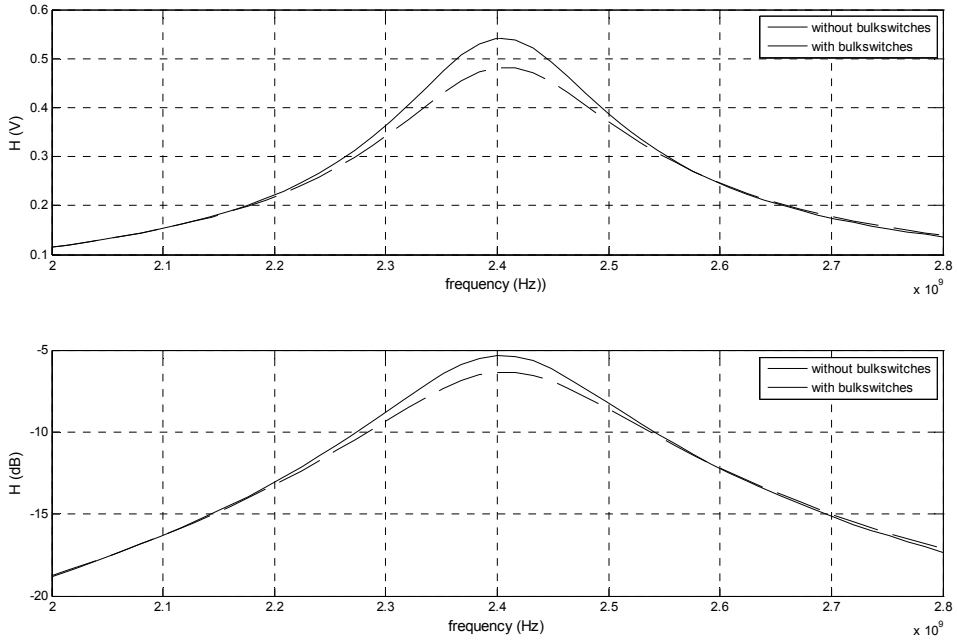

Figure 81 QPAC simulation results of output bandwidth of the quadrature PA with bulkswitches; the dotted, lower line denotes the quadrature pa without bulkswitches

	quadrature PA without bulk switches	**quadrature PA with bulkswitches**
max. magnitude at 2.4GHZ	482 mV -6.34 dB	542 mV -5.89 dB
-3 dB lower sideband bandwidth relative to 2.4 GHz carrier	2.300GHz	2.309GHz
-3 dB lower sideband bandwidth relative to 2.4 GHz carrier	2.519GHz	2.502GHz

Table 17 QPAC simulation numerical output

The QPAC output bandwidth simulation results show that, as shown in the other simulation results, that the quadrature PA with bulkswitches has indeed an higher output amplitude than the quadrature PA without bulkswitches for the same input and input frequency. Besides the difference between the quadrature PA with and

without bulkswitches, it shows a -3dB bandwidth of about f_{3dB}=200MHz, with the bandwidth of the quadrature PA with bulkswitches being slightly larger. This value is quite close to the estimated f_{3dB}=240MHz. Though a smaller bandwidth, corresponding to a higher Q-factor of the LCR tank and thus a steeper curve is desirable to filter out all higher harmonics, it also makes the output amplitude highly dependent of the frequency. Suppose certain output amplitude, which corresponds to a certain input. If the bandwidth curve is steep, a smaller change in input frequency will thus correspond to a bigger change in output amplitude than if the bandwidth curve is less steep.

4.5.5 Power added efficiency performance

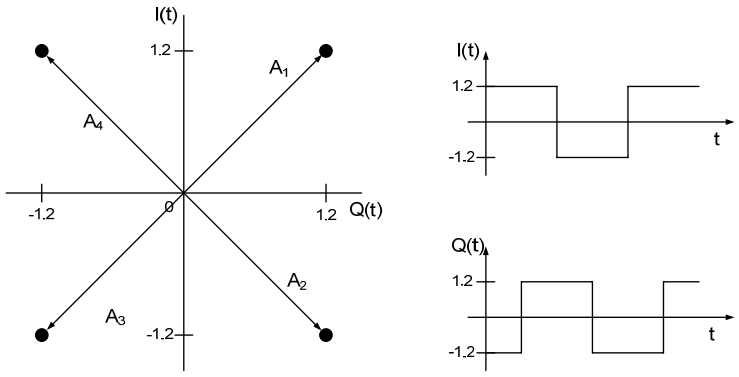

Figure 82 IQ-constellation for PAE simulation

	quadrature PA without bulkswitches		quadrature PA with bulkswitches	
frequency	**PAE**	**output power**	**PAE**	**output power**
10 MHz	31.52 %	6.01 dBm	33.52 %	6.40 dBm
50 MHz	23.86 %	4.80 dBm	24.47 %	5.10 dBm

Table 18 PAE at maximum I(t) and Q(t) input at 10MHz and 50MHz

Table 18 shows the power added efficiency for both the quadrature PA with and without the bulkswitches at maximum input. The quadrature PA with the bulkswitches has a slightly higher PAE, as it has a higher output power. The PAE drops as frequency increases. This is because, as the frequency increases, the output power decreases due to the bandpass characteristic of the LCR filter. Furthermore, the input power is relatively large compared to the output power, about 50% to 60% of the output power. As the frequency increases and the output power drops, the difference between the output and input power becomes smaller, thus decreasing the PAE.

5. Conclusions

A concept for a quadrature power amplifier as alternative to polar power amplifiers using the envelope elimination and restoration linearization technique has been presented. This concept is worked out to a functional model at transistor level.

Simulations show that the quadrature power amplifier is capable of handling quadrature signals operations at RF. Such operations include voltage supply modulation, negative voltage handling, RF carrier multiplying, filtering, power combining and power amplification. A driver has been designed to properly drive the quadrature power amplifier.
The quadrature power amplifier and driver model is designed in 90nm CMOS technology operating at V_{DD}=1.2V and V_{SS}=-1.2V at f_{RF}=2.4GHz. Besides the 90nm feature length devices, larger devices models with a feature length of 240nm were used.

Simulations show that the power added efficiency reach approximately 30% at an output power of 6dBm at maximum input at f_{IQ}=10MHz. and 25% at 5dBm output power at maximum input at f_{IQ}=50MHz

It can be concluded that the presented concept of a quadrature power amplifier indeed is viable. The presented design shows a possible implementation at transistor level. Its power added efficiency show that there is potential as using the quadrature power amplifier as alternative to existing polar power amplifiers.

At time of writing, there is no knowledge of similar research and architecture as presented.

6. Recommendations

The quadrature power amplifier as presented has a maximum output power of about P_{out}=6dBm. For wireless application this is quite low and practical situations would demand a higher output power. To increase the power output, one would lower the load resistance, resulting in a higher current from the supply. Suppose a wanted increase of N-times of power output, N times higher current will be needed, thus an N-times smaller load. To conduct this higher current, all transistor dimensions in the signal path have to scale up N-times as well. To properly drive these bigger transistors, the driver also has to scale up with the same proportions. Possibly also an extra inverter stage will be needed to maintain the drivers step size. Lastly, the LCR filter has to scale as well to tune to the proper Q-factor and frequency. As an addition, using a lower resistance makes it possible to use a N-times smaller inductance, but an N-times increased capacitance, while maintaining the same Q-factor as shown in §3.4.
Since the load has been scaled down, an impedance transformation will be required to transform the output impedance to the 50Ω of the antenna. As suggested in §3.4, a transformer would be suitable. If a transformer is used as impedance transformer, the 50Ω load will be connected to the secondary windings and the output of each half of the bridge connected to the primary winding. The ratio primary to secondary winding will be 1: √N as impedances are transformed by the ratio of the windings squared.

The quadrature PA output is non-linear as the on-resistance of the switches varies with the input, introducing losses and phase shift. This on-resistance behavior is inherent to transmission gate style architectures as used in the quadrature PA. To overcome this non-linearity a different architecture will be needed. Suggested is a classic class-D style architecture consisting of a stacked NMOST and PMOST. Shown in Figure 83, at the left for positive signed I(t) and right for negative signed I(t)

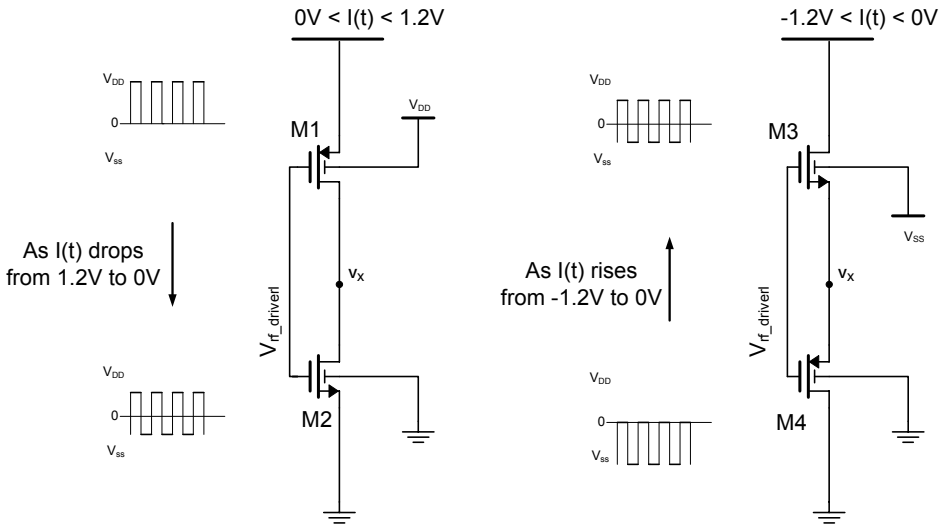

Figure 83 suggested architecture for a quadrature PA to avoid on-resistance non-linearity

Suppose a positive signed I(t). As the quadrature signal input drops, the PMOST will be unable to turn on. To avoid this, the voltage at the gate is “bootstrapped", resulting that the gate voltage drops as well in such a way that the PMOST is still able to turn on. The minimum voltage the driver signal can drop is the minimum voltage which NMOST can still turn on. A same circuit will be needed to provide for a negative signed I(t), shown at the right side of Figure 83, which operates identically only with negative voltages.
The result is an architecture which is not based on transmission gates. The on-resistance is not a combination of the on-resistance of both PMOST and NMOST, but only on either PMOST for positive signed I(t) and NMOST for negative signed I(t). Furthermore, as the gate voltage varies with the source, the gate source voltage varies less, keeping the on-resistance more constant as it is a function of the gate source voltage. Possibly, variation in the threshold voltage can also be reduced by varying the bulk voltage in such a way that it is connected to either the highest or lowest voltage in the system as function of I(t).
However no inverted driver signal is needed anymore, the driver will have to generate a signal which has a DC level, dependent of I(t). Also, two circuits will be needed for one single end quadrature PA. Some sort of switching will be needed to select the proper output of V_X,

A final recommendation is regarding the signal set and the driver. The presented design is heavily restricted by the assumption of the readily available RF signal. With the RF signal being a full swing signal for V_{DD}=1.2V to V_{SS}=-1.2V, the drivers architecture is thus so designed that it also generates the positive switching V_{RF_driver}=0V..1.2V and negative switching V_{RF_driver}=-1.2V..0V, as shown in §3.10.2. To do so, larger, more power consuming 240nm devices are used and the

use of not one, but two inverter chains per driver. Though, one inverter chain is switched off during operation, still the driver consumes relatively much power.
Since the RF signal and the parity bit signals are outputs of most highly likely a digital chip, it is recommended that the generation of the positive and negative switching RF signals and as well the proper switching between these signals takes place in the digital domain. These operations are easily realizable in the digital domain as the RF signals are digital switching signals with all the same frequency. And since no full swing signals is presented at the input of the driver, no thick gate oxide devices are needed in the RF signal path. The result is that both positive as negative switching RF signals are readily available. This implies that the driver can be minimized to just a single chain of inverter as Figure 57 in §3.10.1, but with the first stage consisting of afore mentioned smaller length devices.
Simulation show that such a rearranging of the signal set can increase the PAE up to 27.2% at 5dBm output power at maximum input at f_{IQ}=50MHz. This is an increase of about 10%.

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